High-Bandwidth Dual Active Bridge DC-DC Converter for Data Center Power Management System

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Abstract— **The growing demand for behind-the-meter storage (BTMS) in data centers and high-power EV charging stations calls for compact, reliable, and efficient power conversion solutions. To meet these requirements, the Dual Active Bridge (DAB) converter topology is chosen for its inherent soft-switching capability, enabling high efficiency and superior power density. In data center applications, where dynamic load variations are common, achieving high-bandwidth control is essential for stable operation. A critical factor influencing this bandwidth is the selection of the DC-link capacitor, which directly impacts system performance. This paper investigates the complex interplay between input and output DC-link capacitance and its effect on bandwidth in DAB converters. Through state-space modeling and state-variable feedback control, the proposed design and control approach is validated on a 2 kW DAB prototype, demonstrating improved bandwidth without compromising ripple performance.**

Keywords—High bandwidth control, Datacenter, GaN, DAB, State space modeling, State variable feedback control, BTMS, DC-DC converter.

I. INTRODUCTION

The exponential growth of cloud computing, artificial intelligence, machine learning, and data-driven applications has led to an unprecedented increase in data center power consumption [1], [2]. As modern data centers strive to support exascale computing while maintaining performance and speed, power infrastructure must evolve to handle rising loads without compromising efficiency or thermal management [3]. Behind-the-meter storage (BTMS) is gaining importance to facilitate grid integration under these growing electrical demands. Consequently, the combined demand for efficient, high-power-density DC-DC conversion architecture has surged to meet these computing and EV charging requirements.

Among the various DC-DC converter topologies, the Dual Active Bridge (DAB) converter has emerged as a leading solution for isolated DC-DC power conversion in data centers and high-power EV charging applications due to its ability to deliver high efficiency and superior power density [4]. In rack- or server-level power supplies, where energy efficiency directly impacts operational costs and thermal management [5], the DAB topology offers distinct advantages, as illustrated in the example architecture shown in Fig. 1. This architecture employs a ±400 V DC bus for high-voltage distribution while supporting an inner 48 V DC bus for legacy equipment. Although variations of ±400 V based DC distribution architectures exist for compute racks or side-car racks [6], [7].

DAB converters provide inherent benefits such as galvanic isolation, soft-switching capability, and a symmetric structure, making them well-suited for distributed power architecture, BTMS, and hybrid energy systems in both edge and centralized data centers [8]. Furthermore, their ability to operate efficiently across wide load and voltage ranges enables flexible integration into modular power supplies and redundancy systems. The adoption of wide-bandgap (WBG) semiconductor devices, particularly gallium nitride (GaN) transistors, has further enhanced converter performance [9], [10]. Compared to conventional silicon MOSFETs or IGBTs, GaN devices offer superior switching characteristics, higher breakdown voltage, and lower gate charge, significantly reducing switching losses [11]-[12].

High-bandwidth DC-DC converters are essential for maintaining stability in sensitive systems by providing rapid response to load or input variations. These converters deliver fast transient response, improved regulation, and enhanced efficiency. Additionally, high-bandwidth current synthesis facilitates rapid performance evaluation, testing, and system level interaction. While numerous studies have addressed high-bandwidth controller design for DC-DC converters [13], its application to DAB converters remains relatively unexplored. Existing modeling and control approaches are discussed in [14], yet the relationship between system bandwidth and filter design for DAB converters has not been thoroughly investigated. Previous work on full-order continuous-time models using generalized average modeling focuses on AC transformer currents [15], neglecting dynamic effects. This paper instead emphasizes an intuitive representation of bandwidth dependence on system parameters and explores volumetric downsizing through additional filtering stages without sacrificing bandwidth an approach particularly relevant for aerospace applications [16]- [18].

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In this work, a reduced-order state-space model is developed, and a closed-loop controller is designed to evaluate the impact of DC-link capacitor selection on system bandwidth. Model accuracy is verified by comparing the open-loop step response of the state-space model with that of the circuit-level model. Subsequently, closed-loop bandwidth is assessed through frequency response analysis. By incorporating a harmonic trap filter, ripple current is mitigated, enabling a reduction in DC-link capacitance while achieving higher bandwidth. The proposed design achieves a target bandwidth of 5 kHz, with total harmonic distortion (THD) used as a metric for ripple current estimation.

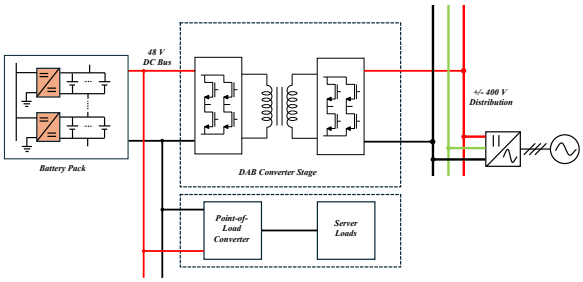


Fig. 1: Example power flow diagram for a single datacenter rack.

II. Dual Active Bridge Converter Modeling

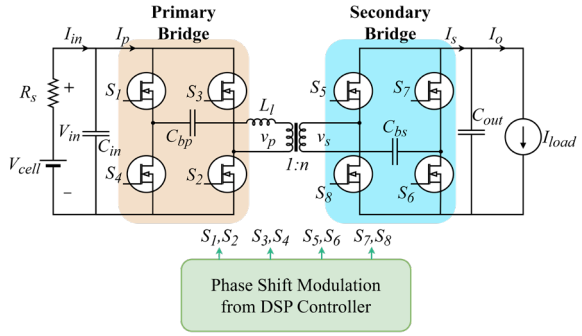


Fig. 2. Generic DAB converter [1]

Developing an overall system model of the DAB converter is essential for achieving the desired bandwidth and ensuring optimal performance. To accomplish this, a simplified reduced-order modeling approach is adopted, which omits the detailed dynamics of the transformer current. This simplification reduces complexity while preserving the key characteristics of the system, as described in [14]. In this model, the primary and secondary bridges of the DAB converter are represented as dependent current sources, accurately capturing power transfer between the two sides. These sources are mathematically defined in Equations (1) and (2). By using dependent current sources, the representation of power flow becomes more intuitive, enabling efficient analysis of system behavior under varying operating conditions. Fig. 2 illustrates the schematic of a generic DAB converter, while Fig. 3 presents the reduced-order model, clearly depicting the relationships between the primary and secondary circuits. This model serves as the foundation for subsequent control system design and analysis.

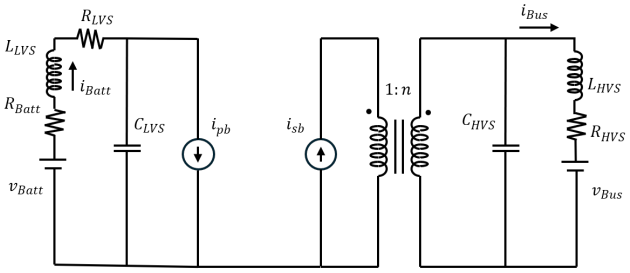


Fig. 3. DAB converter reduced-order model

$$i_{pb} = \frac{d(1-d)v_{BUS}}{2f_{sw}nL_t} \tag{1}$$

$$i_{sb} = \frac{d(1-d)v_{Batt}}{2f_{sw}nL_t} \tag{2}$$

Where, i_{pb} and i_{sb} are the primary and secondary bridge average current respectively, single-phase shift (SPS) modulation is employed between the primary and secondary bridges, denoted as d. The switching frequency is f_{sw} [Hz], the transformer leakage inductance is L_t [H], and the transformer turns ratio is n. The state equations are derived below,

$$L_{LVS}\frac{di_{Batt}}{dt} = v_{Batt} - i_{Batt}(R_{Batt} + R_{LVS}) - v_{C_{LVS}} \tag{3}$$

$$C_{LVS}\frac{dv_{C_{LVS}}}{dt} = i_{Batt} - \frac{d(1-d)v_{Bus}}{2nf_{sw}L_t} \tag{4}$$

$$L_{HVS}\frac{di_{Bus}}{dt} = v_{C_{HVS}} - R_{HVS}i_{Bus} - v_{Bus} \tag{5}$$

$$C_{HVS}\frac{dv_{C_{HVS}}}{dt} = \frac{d(1-d)v_{Batt}}{2nf_{sw}L_t} - i_{Bus} \tag{6}$$

$$\dot{x} = \begin{bmatrix} -(R_{Batt}+R_{LVS})/L_{LVS} & -1/L_{LVS} & 0 & 0 \\ 1/C_{LVS} & 0 & 0 & 0 \\ 0 & 0 & -R_{HVS}/L_{HVS} & 1/L_{HVS} \\ 0 & 0 & -1/C_{HVS} & 0 \end{bmatrix} + \begin{bmatrix} 1/L_{LVS} & 0 \\ 0 & -\frac{d(1-d)}{2nf_{sw}L_tC_{LVS}} \\ 0 & -1/L_{HVS} \\ \frac{d(1-d)}{2nf_{sw}L_tC_{HVS}} & 0 \end{bmatrix} u \tag{7}$$

The large-signal state-space model, shown in Equation (7), is derived from the state equations (3–6) and exhibits nonlinearity with respect to the control input phase shift, d. To enable effective analysis and controller design, the model is linearized using the small-signal perturbation method. In this process, system states and inputs are expressed as the sum of their steady-state (DC) and perturbation (AC) components, as described in [16]. During linearization, DC terms and higher-

order components are neglected, resulting in the simplified small-signal model presented in Equation (8).

$$\dot{\tilde{x}} = \begin{bmatrix} -(R_{Batt}+R_{LVS})/L_{LVS} & -1/L_{LVS} & 0 & 0 \\ 1/C_{LVS} & 0 & 0 & 0 \\ 0 & 0 & -R_{HVS}/L_{HVS} & 1/L_{HVS} \\ 0 & 0 & -1/C_{HVS} & 0 \end{bmatrix} \tilde{x} + \begin{bmatrix} 0 \\ \frac{-(1-2D)V_{Bus}}{2nf_{sw}L_tC_{LVS}} \\ 0 \\ \frac{(1-2D)V_{Batt}}{2nf_{sw}L_tC_{HVS}} \end{bmatrix} \tilde{d} \quad (8)$$

The derived small-signal model is intended to enable control of both the server current and the bus current. However, since the primary objective is server current regulation, the system can be effectively decoupled, simplifying the dynamics and reducing the system order. The dynamic response of the battery side current to a step change in phase shift has been validated through simulation. Fig. 4 illustrates the transient response, with simulation parameters summarized in Table I. These results confirm that the proposed model accurately captures system behavior, supporting its suitability for achieving the desired control objectives.

In Fig. 4, the circuit model's step response exhibits ripple at 400 kHz, corresponding to the 200 kHz switching frequency. The observed settling time and overshoot are approximately 70 µs and 5%, respectively. The step responses of the circuit model and the small-signal model closely align, further validating the accuracy of the reduced-order representation.

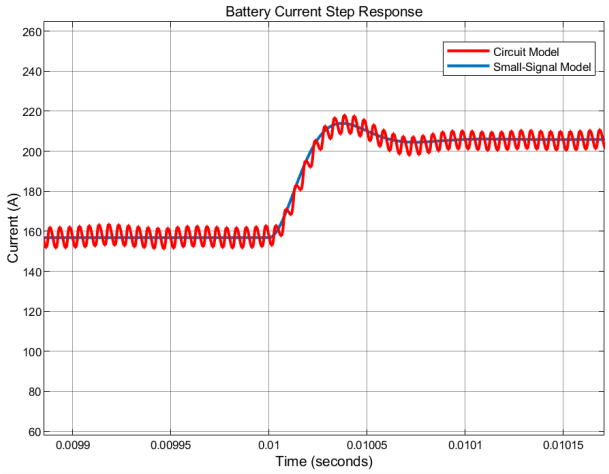


Fig. 4. Server current step response circuit model vs small-signal model

TABLE I. CONVERTER SPECIFICATION

Parameter	Value
Nominal Battery Voltage ($V_{Batt-nom}$)	48 V
DC Bus Voltage (V_{Bus})	400 V
Transformer Turns Ratio (n)	1:8
Switching Frequency (f_{sw})	200 kHz
Rated Power (P_{rated})	2 kW
HVS DC-Link Capacitance (C_{HVS})	560 µF
HVS Leakage Inductance (L_t)	14.55 µH
LVS Cable Resistance (R_{LVS})	0.213 mΩ
LVS Cable Inductance (L_{LVS})	105.33 nH
HVS Cable Resistance (R_{HVS})	1.6 mΩ
HVS Cable Inductance (L_{HVS})	344 nH

III. STATE VARIABLE FEEDBACK CONTROLLER DESIGN

The controller and hardware design are guided by two key objectives: achieving a target bandwidth of 5 kHz and maintaining server current THD below 1%. To improve the system's dynamic performance, a state-variable feedback control strategy is implemented. However, due to the system's characteristics, an integrator is added to eliminate steady-state error. The closed-loop control structure is illustrated in Fig. 5.

Frequency response analysis of the closed-loop system considering only state-variable feedback reveals that increasing the DC-link capacitance has a significant effect on system bandwidth. This insight is critical for optimizing both control performance and component selection.

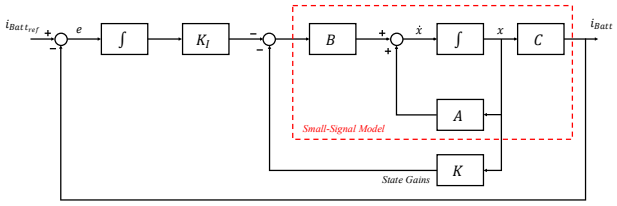


Fig. 5. Closed-loop system block diagram

The results in 6 highlight a key trade-off in system performance. Fig. 6 shows that increasing the DC-link capacitance reduces system bandwidth, due to the capacitor's greater energy storage, which slows the system's dynamic response.

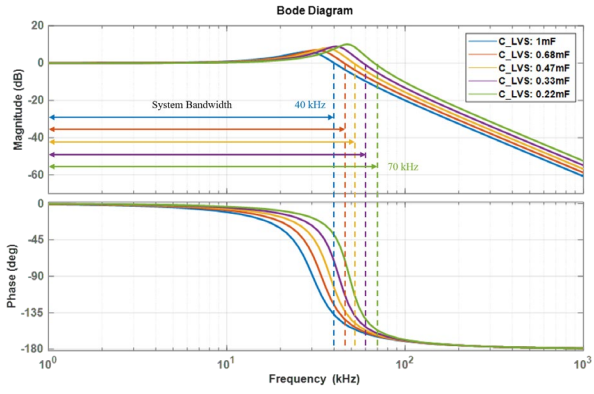


Fig. 6. Closed-loop system frequency response for varying DC-link capacitor values

To mitigate ripple current in the server, this study introduces a harmonic trap filter design. The primary objective of this filter is to reduce the required DC-link capacitance by attenuating the dominant harmonic component in the server current. This approach not only minimizes the need for large capacitors but also supports achieving the desired system bandwidth while reducing current ripple. The server current contains a 400 kHz ripple, originating from the converter's 200 kHz switching frequency. To suppress this high-frequency component, a harmonic trap filter is implemented. Designed as an LC resonant tank circuit, shown in Fig. 7, the filter is precisely tuned to target and eliminate the 400 kHz harmonic. This results in improved current quality and reduced harmonic distortion, thereby enhancing overall system performance.

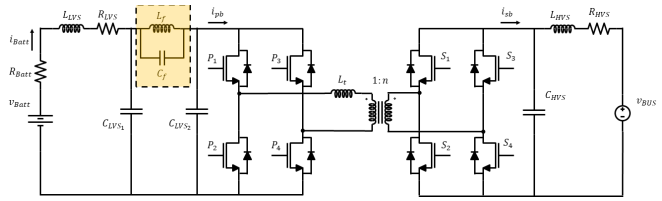


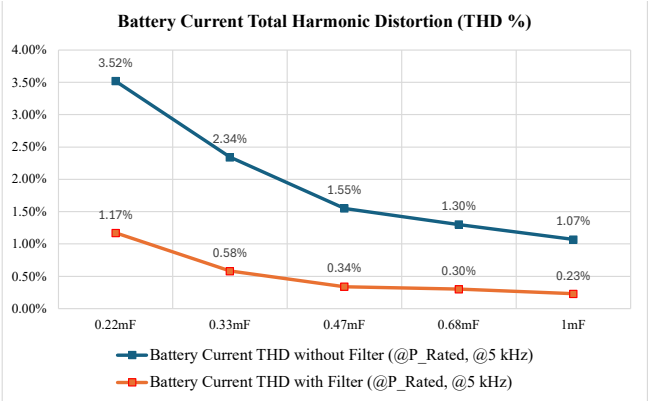
Fig. 7. DAB with LC trap filter at the server side

The relation between trap filter resonance frequency, f_r and the filter capacitance, C_f and inductance, L_f can be expressed using the following equation (9). From (9) the required capacitance and inductance to attenuate 400 kHz harmonic is calculated.

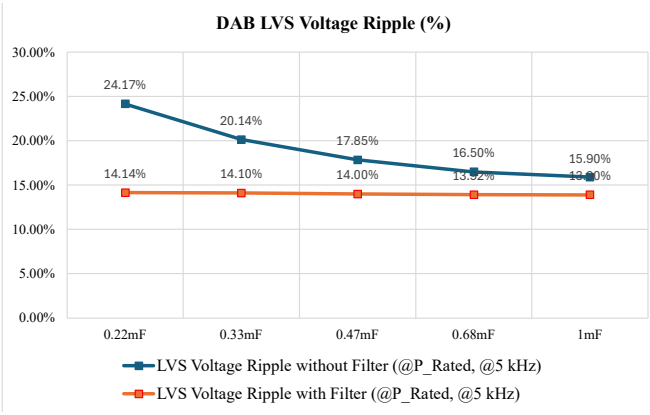
$$f_r = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{9}$$

The implementation of the harmonic trap filter has led to a marked improvement in the system's harmonic performance, particularly in reducing THD in the server current. This enhancement in current quality is achieved without increasing the DC-link capacitance, thereby avoiding additional strain on the system's passive components. Moreover, the voltage ripple at the LVS remains unaffected, as shown in Fig. 8(a) and (b), ensuring output voltage stability under the new filtering conditions.

Further insight into the system's dynamic behavior is provided by the open-loop pole-zero analysis shown in Fig. 9. From Fig. 9, the harmonic trap filter introduces two additional poles to the system which increase system dynamic response and reduce the requirement of the bulky capacitor. The addition of the harmonic trap filter not only suppresses high-frequency distortion but also contributes to improved system dynamics. The modified pole-zero placements indicate enhanced stability margins and faster transient response. As a result, the proposed filter design not only fulfills its primary goal of harmonic attenuation but also strengthens the overall robustness and efficiency of the converter system.



(a)



(b)

Fig. 8. (a) Battery/ Server Side current THD; (b) DAB LVS voltage ripple -for varying DC-link capacitor values with and without trap filter

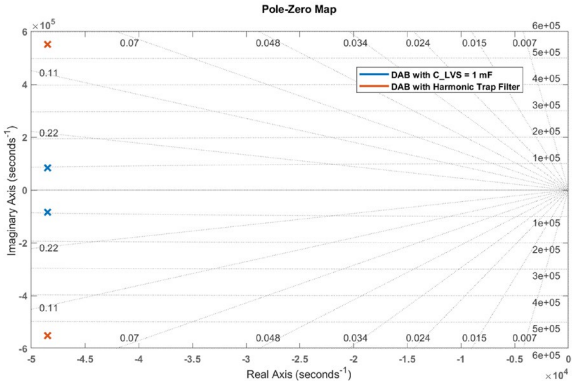


Fig. 9. Open-loop system's pole-zero map with trap filter (red) and without trap filter (blue)

IV. Simulation Results

A preliminary efficiency evaluation of the DAB stage was conducted with shown prototype in Fig. 10 for power transfer from the 48 V DC bus to the 400 V DC bus, with a resistive load connected at the high-voltage side. The DAB stage achieved a peak efficiency of 97.8% while processing up to 2 kW of power as represented in Fig. 11. Another key

performance metric is the system's emulation capability at the low-voltage bus. A periodic current profile test was conducted at various magnitudes and frequencies, demonstrating that the system can effectively synthesize different current waveforms up to 5 kHz. As shown in Fig. 12, a 15 A sinusoidal waveform was accurately reproduced at 5 kHz. In addition, triangular and sawtooth waveforms were synthesized at 1 kHz and 250 Hz, respectively, each with amplitudes of approximately 6.5 A, as illustrated in Fig. 13 and 14 respectively.

Fig. 10. Prototyped DCE Hardware

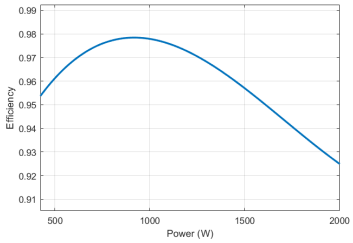


Fig. 11. DCE DAB Stage Efficiency

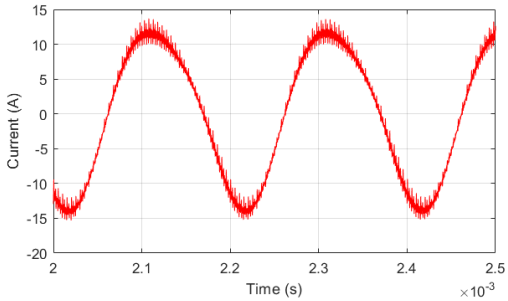


Fig. 12. A sinusoidal current waveform (15 A peak, 5 kHz)

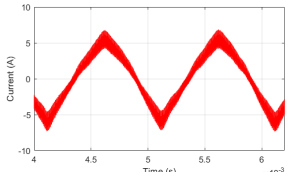


Fig. 13. A triangular current waveform (6.5 A peak, 1 kHz)

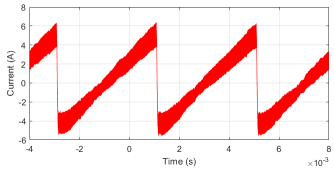


Fig. 14. A sawtooth current waveform (6.5 A peak, 250 Hz)

V. Conclusions

In conclusion, this work demonstrates the successful implementation of high-bandwidth control for a DAB converter through reduced-order state-space modeling and state-variable feedback control. The study underscores the critical influence of DC-link capacitor selection on system bandwidth, highlighting the importance of precise design for applications with stringent performance requirements, such as datacenter power management systems. To overcome the challenge of achieving the target bandwidth while minimizing bulky DC-link capacitance, a harmonic trap filter is integrated into the design. This approach significantly improves system response and enables downsizing without compromising performance. The proposed methodology combining simplified continuous-time modeling with advanced control has been validated through simulations on a 2 kW DAB converter. Results confirm the effectiveness of the strategy, demonstrating its potential for practical deployment in datacenter applications.

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