A Multi-State Adaptive Virtual Impedance Controller for Fault-Responsive Heterogeneous Parallel GFMs

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***Abstract*—This paper presents a unified control framework for Grid-Forming Inverters (GFMIs) that simultaneously addresses two longstanding challenges: reliable overcurrent limiting and enhanced transient stability. The proposed Multi-State Adaptive Virtual Impedance (AVI) dynamically adjusts its resistive to reactive characteristics across three operating states: Normal Operation (ST0), Fault-Limiting (ST1), and Post-Fault Recovery (ST2). In ST0, a decentralised, consensus-based current-difference controller tunes the AVI to ensure accurate power sharing and suppress circulating currents among heterogeneous parallel GFMIs. Upon fault detection (ST1), the AVI transitions to a predominantly reactive profile to enforce output-current limitation to the inverter's short-term rating while preserving grid-forming voltage-source behaviour, avoiding instability caused by GFM-GFL mode switching. After fault clearance (ST2), the AVI adopts a high-resistive profile to provide active damping, suppress power oscillations, and enhance first-swing stability. The proposed multi-state framework ensures robust coordination and stability across all grid conditions and is validated through detailed MATLAB/Simulink simulations.**

***Index Terms*--Adaptive Virtual Impedance (AVI); Fault Ride-Through (FRT); Grid-Forming Inverters (GFMIs); Overcurrent Limiting; Transient Stability Enhancement.**

I. INTRODUCTION

The transition from conventional power systems dominated by synchronous generators (SGs) to future grids with high penetrations of inverter-based resources (IBRs) is well underway. In this new paradigm, GFMIs are emerging as a critical technology to replace the foundational grid services, such as inertia and voltage/frequency stability, previously supplied by SGs [1]. GFMIs achieve this by operating as controlled voltage sources behind a virtual impedance, intrinsically regulating the voltage and frequency at their terminals [2], [3].

This voltage-source behaviour, however, presents a profound challenge. Unlike SGs, which possess high thermal mass and can supply 5-6 p.u. fault currents, power electronic inverters have minimal thermal overload capacity. Their hardware (e.g., IGBTs) must be protected by fast-acting current-limiting controls, typically restricting the output to an Inverter Short-term Rated Current (ISRC) of 1.2–1.5 p.u. [4], [5]. This creates a fundamental conflict between the GFM's control objective (maintain a stable voltage) and its physical limitations (protect hardware from overcurrent).

The very act of limiting the current, especially through common methods like hard saturation or switching to a grid-following (GFL) current-source mode, fundamentally breaks the GFM's power-synchronisation loop. This transition can cause the converter to transiently lose synchronisation, leading to angle-stability issues and failed post-fault recovery [4].

Existing solutions that employ virtual impedance (VI) to manage fault currents fall into an intractable trade-off.

1. **Resistive VI ($R_v >> X_v$):** This configuration is highly effective at damping the transient DC component of the fault current [5], [6] and is essential for damping post-fault power oscillations [7]. However, as identified in [1], a highly resistive source impedance "conflicts with the requirements of protective relays," which are often designed to see a "highly inductive" source for reliable operation of supervising elements.
2. **Reactive VI ($X_v >> R_v$):** This configuration satisfies the protection-interoperability requirement but provides poor damping for transient DC currents and, more critically, does not provide active damping for post-fault power angle oscillations [8].

Furthermore, these challenges are compounded in systems with multiple *heterogeneous* parallel GFMIs [9]. Mismatches in inverter ratings, filter impedances, and control parameters render simple droop control ineffective, leading to poor power sharing and large circulating currents that compromise efficiency and reliability [10], [11].

This paper resolves these multifaceted challenges by proposing a unified, Multi-State AVI framework. This controller functions as a "control chameleon," dynamically reconfiguring its R/X ratio and control objective based on three distinct, locally-measured operating states:

1. ST0 (Normal Operation): A low-frequency adaptive VI ensures accurate power sharing and suppresses circulating currents.

2. ST1 (Fault-Limiting): The AVI transitions to a predominantly *reactive* VI (AVI-Rxt) for current limiting.

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3. ST2 (Post-Fault Recovery): The AVI transitions again to a predominantly *resistive* VI (AVR) to provide active power oscillation damping.

This single, unified GFM control strategy ensures stability, protection-interoperability, and coordination across all operating conditions without compromise.

II. Problem Statement and Limitations of Existing Strategies

A. The GFM Fault-Response Trilemma: Protection, Damping, and Stability

The core control loop of a GFMI calculates a voltage reference (v^*) to be synthesised by the converter. During a fault, the grid voltage at the point of common coupling (PCC), v_{pcc}, collapses. The resulting current, $i = (v^* - v_{\text{pcc}})/(Z_{\text{line}} + Z_{\text{filter}})$, is driven by a large voltage differential across a low impedance, demanding a current that far exceeds the ISRC. This forces the controller into one of three conflicting objectives: hardware protection, stability maintenance, or protection-system coordination.

1) Limitation 1: Saturation and Mode-Switching (The Stability Conflict)

The most common solution is to saturate the current reference or switch the control from a voltage-source (GFM) to a current-source (GFL) mode [4], [5]. This action is inherently destabilising. As highlighted in [4], the transition to a current-source mode for saturation "has the potential for the converter to transiently lose synchronisation." This occurs because the saturation or mode-switch "breaks" the power-synchronisation loop that ties the inverter's internal angle δ to its power output. The GFM controller effectively becomes "blind," causing its internal angle to drift, which leads to integrator windup and prevents successful resynchronisation after the fault is cleared [7], [12].

2) Limitation 2: The Virtual Impedance R/X Contradiction (The Protection & Damping Conflict)

Using a static virtual impedance $Z_v = R_v + jX_v$ to limit the fault current presents a fundamental and previously unresolved contradiction in the required R/X ratio.

- **The Case for Resistive VI ($R_v \gg X_v$):** A resistive impedance is highly desirable for damping. It effectively accelerates the decay of the "attenuated DC component" of the fault current [6]. In the post-fault recovery phase, a virtual resistor is the primary tool for injecting active damping to quell power oscillations [7].
- **The Case for Reactive VI ($X_v \gg R_v$):** Power system protection, particularly supervising elements in directional and phase-selection relays, is designed for the high *X/R* ratio fault characteristics of SGs. As detailed in [1], a control-based VI used for current limiting, "should be highly inductive" to ensure the reliability of these relays. Incorporating virtual resistance "conflicts with the requirements of protective relays".

This creates an intractable trade-off: a static VI must choose between *transient current damping* and *protection interoperability*. No single static *R/X* ratio is optimal for both the fault-limiting phase (ST1) and the post-fault damping phase (ST2). The plot in Figure 1 illustrates the Multi-State AVI mechanism, showing how the virtual resistance (R_v) dynamically adjusts based on the operating state. In Normal Operation, R_v is low. When the output current (I_{out}) exceeds the Nominal Current (I_n), the controller enters the Fault-Limiting mode (ST1), where R_v quickly rises to enforce current limiting. This rapid adaptation ensures robust stability and overcurrent protection for the GFMI.

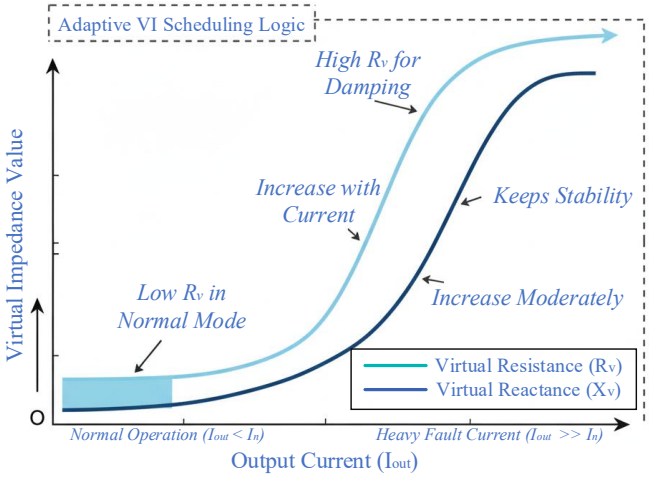

Figure 1. AVI qualitative behaviour

TABLE I. Comparative Analysis of Existing GFMI Fault-Ride-Through Techniques

Strategy	Current (I≤ISRC) Limiting	Maintains GFM Behavior (Voltage Source)	Protection-Relay Interoperable (High Xv)	Damps Oscillations & DC Current (High Rv)	Manages Heterogeneous Parallel Operation (CC Suppression)
GFM-to-GFL Mode Switch	Yes	**No** [5], [16]	N/A	No	No
Current Saturation Limiter	Yes	**No** (Loses sync) [17]	N/A	Poor	No
Static Resistive VI	Yes	Yes	**No** [1]	Yes	Poor
Static Reactive VI	Yes	Yes	Yes [1]	**Poor** [1]	Poor
Proposed Multi-State AVI	**Yes**	**Yes**	**Yes (ST1)**	**Yes (ST2)**	**Yes (ST0)**

3) Limitation 3: The Heterogeneity Conflict (The Coordination Conflict)

Modern power networks increasingly deploy heterogeneous parallel GFMI systems, where multiple grid-forming inverters operate together under diverse configurations and dynamic conditions [9]. In such systems, GFMIs with different MVA ratings, *Z/R* ratios, and control parameters (e.g., VSG vs. droop) are paralleled. Simple droop control is insufficient to manage

these asymmetries, resulting in poor reactive power sharing and, more critically, large low-frequency (LF) and high-frequency (HF) zero-sequence circulating currents (ZSCCs) [13]. These currents consume inverter capacity, increase losses, and threaten system reliability [14], [15]. Existing methods for CC suppression are typically designed as add-ons, separate from the fault-ride-through (FRT) control logic.

A comparative analysis of existing FRT techniques, summarised in Table 1, highlights the clear gap in the literature. No single existing strategy can simultaneously limit current, maintain GFM behaviour, ensure protection interoperability, provide active damping, and manage heterogeneous operation.

III. Proposed Multi-State Adaptive Virtual Impedance (AVI) Controller

A. Unified Control Architecture and State-Transition Logic

The proposed AVI controller is not a collection of three independent controllers but a single, unified virtual impedance, $Z_{AVI}(s)$, embedded within the GFM inverter's voltage reference calculation. Figure 2 shows the simplified version of the proposed system architecture. The core architecture is based on the standard GFM voltage reference generation:

$$v^*_{\text{ref}} = v^*_{GFM} - Z_{AVI} \cdot i_{\text{out}} \quad (1)$$

where v^*_{GFM} is the internal voltage reference from the GFM primary controller (e.g., droop or VSG), and i_{out} is the measured output current. The innovation lies in the state-transition logic that algorithmically re-parameterises the composition of $Z_{AVI} = R_v + jX_v$ in real-time based on locally measured grid conditions.

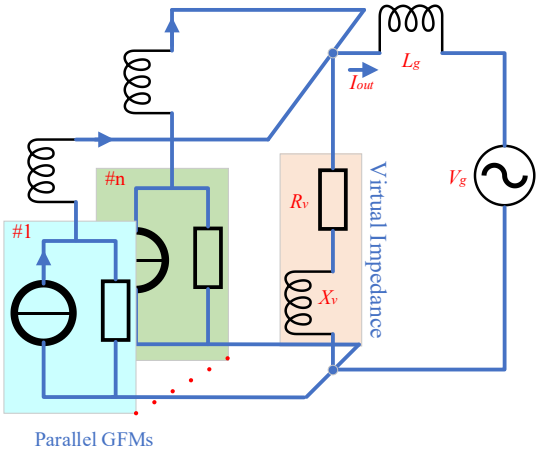

Figure 2. Simplified proposed system configuration

To ensure robustness and avoid communication requirements, the controller's logic is decentralised and relies only on local measurements at the inverter's terminals. A state machine, structured in line with established GFMI transition-logic frameworks, orchestrates the controller's behaviour.

State Definitions:

- **ST0 (Normal Operation):** This is the default state when the system is stable. The trigger is $v_{pcc} > 0.85$ *p.u*
- **ST1 (Fault-Limiting):** This state is entered immediately upon fault detection, defined by a significant voltage sag, $v_{pcc} \leq 0.85$ *p.u.*.
- **ST2 (Post-Fault Recovery):** This state is triggered when the fault is cleared, detected by the PCC voltage recovering (v_{pcc} rises above 0.85 p.u.). This state remains active for a predefined time T_{damp} or until the inverter's active power output P_{rec} recovers to a set threshold (e.g., $P_{rec} > 0.8 \cdot P_{ref}$), indicating the initial power-angle swing has been stabilised.

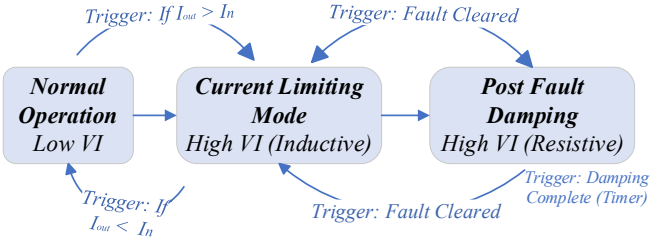

Figure 3. GFMI Adaptive VI: Multi-State Transition Diagram

Figure 2 is a Multi-State Transition Diagram for the GFMI's AVI logic. It shows three operating states: Normal Operation (low VI), Current-Limiting Mode (high, inductive VI), and Post-Fault Damping (highly resistive VI). Transitions are triggered by the output current (I_{out}) relative to the Nominal Current (I_n) or by the detection/clearing of a fault, which are described in detail in the subsequent subsection.

B. ST0 (Normal Operation): Adaptive Power Sharing Control

In ST0, Z_{AVI} is designed to address the "Heterogeneity Conflict". The goal is to ensure accurate, rating-proportional power sharing and suppress circulating currents (CCs) between the parallel GFMIs.

1) Low-Frequency (LF) CC Suppression:

To ensure accurate active and reactive power sharing and suppress LF circulating currents caused by mismatched impedances, a consensus-based current-difference controller is used. This adds a PI controller ($G_c(s) = K_{pc} + K_{ic}/s$) that modifies the inverter's reference current based on the difference from its neighbours, effectively creating an adaptive virtual impedance that drives imbalances to zero. The control law modifies the original current references (I_{refd}, I_{refq}) generated by the outer GFM loops, as derived:

$$I^*_{\text{refd1}} = I_{\text{refd1}} - G_c(s) \cdot (I_{d1} - I_{d2}) \quad (2)$$

$$I^*_{\text{refd2}} = I_{\text{refd2}} - G_c(s) \cdot (I_{d2} - I_{d1}) \quad (3)$$

2) High-Frequency (HF) CC Suppression:

To suppress HF zero-sequence circulating currents (ZSCCs) caused by PWM mismatches, a virtual inductor L_v is implemented. In the *d-q* frame, this requires implementation of the derivative $p = d/dt$ and the cross-coupling terms:

$$v^*_{d,\text{ref}} = v^*_{d,GFM} - (L_v p \cdot i_d - \omega L_v \cdot i_q)$$
$$v^*_{q,\text{ref}} = v^*_{q,GFM} - (L_v p \cdot i_q + \omega L_v \cdot i_d) \quad (4)$$

C. ST1 (Fault-Limiting): Adaptive Virtual Reactance (AVI-Rxt)

Upon detecting a fault (ST1), the ST0 controller is disengaged. The objective is to limit the output current I_s to the Inverter Short-term Rated Current (I_{ISRC}) while maintaining GFM behaviour. This is achieved by implementing Z_{AVI} as an adaptive impedance $Z_{vadp} = R_{vadp} + jX_{vadp}$. The magnitude is adaptively scaled based on the measured current $I_s = \sqrt{i_d^2 + i_q^2}$ relative to the rated current I_n.

$$R_{\text{vadp}} = \begin{cases} 0 & \text{if } I_s \le I_n \\ k_R(I_s - I_n) & \text{if } I_s > I_n \end{cases} \quad (5)$$

To ensure interoperability with protective relays, the impedance is made predominantly reactive by setting a high virtual impedance ratio $\sigma = \frac{X_{\text{vadp}}}{R_{\text{vadp}}}$ (e.g., e.g., σ = 10). The adaptive reactance is then:

$$X_{\text{vadp}} = \sigma \cdot R_{vadp} \quad (6)$$

This Z_{vadp} is injected into the voltage reference equations, creating a "soft" current limit that avoids controller saturation:

$$v^*_{d,\text{ ref}} = v^*_{d,GFM} - \left(R_{vadp} \cdot i_d - X_{vadp} \cdot i_q\right) \quad (7)$$

$$v^*_{q,\text{ ref}} = v^*_{q,GFM} - \left(R_{vadp} \cdot i_q + X_{vadp} \cdot i_d\right) \quad (8)$$

D. ST2 (Post-Fault Recovery): Adaptive Virtual Resistor (AVR)

Once the fault clears (ST2), the ST1 controller is disabled. The objective flips from current limiting to actively damping the post-fault power-angle oscillations.

Z_{AVI} now becomes a pure Adaptive Virtual Resistor (AVR), $Z_{AVI} = R_v(t)$. This resolves the R/X conflict by applying high resistance only when needed for damping. The resistance value is made "adaptive to the recovery rate" of the VSC by making it proportional to the magnitude of the rate of change of filtered active power, P_{filt}:

$$R_v(t) = K_{\text{avr}} \cdot \left|\frac{d}{dt} P_{\text{filt}}\right| \quad (9)$$

This adaptive $R_V(t)$ injects active damping proportional to the oscillation's velocity, rapidly stabilising the inverter. The voltage reference equations become:

$$v^*_{d,\text{ ref}} = v^*_{d,GFM} - \left(R_v(t) \cdot i_d\right)$$

$$v^*_{q,\text{ ref}} = v^*_{q,GFM} - \left(R_v(t) \cdot i_q\right) \quad (10)$$

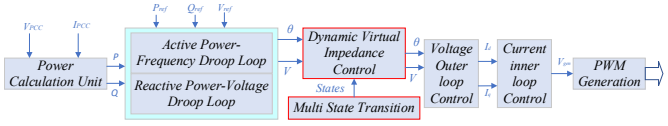

Figure 4. GFMI multi-loop control block diagram with AVI

Figure 4 presents the Multi-Loop control block diagram for the GFMI featuring AVI. The control structure includes the Outer Voltage/Droop Loop for power reference tracking and the Inner Current Loop for current regulation. The AVI block integrates into the voltage reference path to dynamically adjust the output impedance for overcurrent limiting and stability across various operating conditions.

IV. Simulation Results and Analysis

The proposed Multi-State AVI controller is evaluated using a detailed MATLAB/Simulink model comprising two heterogeneous grid-forming inverters (GFM1: 4×10⁶ VA, GFM2: 6×10⁶ VA) operating in parallel at a common PCC. The simulations assess steady-state coordination, fault-current limiting, post-fault recovery, and reconnection behaviour across the three operating states (ST0–ST2). The following results demonstrate the controller's effectiveness in ensuring accurate power sharing, robust fault response, and stable recovery under representative grid disturbances.

A. Case 1: Normal Operation (ST0) – Power Sharing & Circulating-Current Suppression

Under normal operating conditions (ST0), the proposed AVI ensures accurate rating-proportional power sharing between the heterogeneous parallel GFMIs while suppressing both low-frequency and high-frequency circulating currents. Fig. 5 illustrates the system response to a step change in the active-power reference of GFM1. Following the reference update, both converters smoothly converge to the new sharing ratio without overshoot or distortion, and the inverter currents remain well-balanced throughout the transient. The result confirms that the consensus-based current-difference controller embedded in the ST0 logic successfully mitigates circulating current components, enabling stable active power redistribution even under heterogeneous filter and controller parameters.

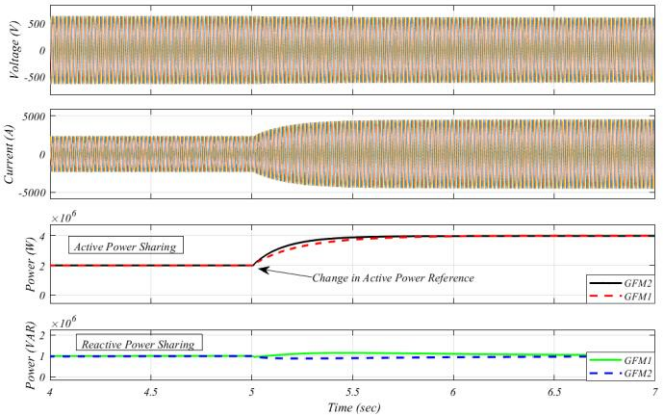

Figure 5. Active-power sharing response under normal operation following a step change

B. Case 2: Three-Phase Fault (ST1 & ST2) – Current Limiting & Recovery, Reconnection (ST0) & Inrush Suppression

Fig. 6 presents the system response during a three-phase fault when only a predominantly resistive virtual impedance is used. Immediately after the ST0 → ST1 transition, the inverter currents exhibit a pronounced overcurrent peak of approximately 3.1–3.4 p.u., exceeding the rated ISRC. The lack of reactive shaping during ST1 results in poor current limitation and a distorted PCC voltage waveform. After fault clearance (ST1 → ST2), the system experiences significant first-swing angle instability, with frequency excursions exceeding ±1.2 Hz, and the post-fault active damping is insufficient to stabilise oscillatory power exchange. The system requires nearly 200–250 ms to settle back to ST0 conditions, and residual

oscillations remain observable, indicating inadequate damping and susceptibility to desynchronisation during recovery.

In contrast, Fig. 7 demonstrates the proposed Multi-State Adaptive Virtual Impedance (AVI) behaviour. During ST1, the adaptive virtual reactance limits the peak fault current to within 1.25–1.35 p.u., ensuring hardware-safe operation while preserving GFM behaviour without mode switching. The PCC voltage distortion is substantially reduced, reflecting improved protection interoperability due to the high-X AVI profile. Upon transitioning to ST2, the adaptive virtual resistor injects transient active damping, visibly suppressing the post-fault oscillations within 80–100 ms, reducing the frequency nadir deviation to within ±0.35 Hz. During the ST2 → ST0 reconnection phase, the proposed controller effectively mitigates inrush currents, and the voltage and current waveforms resynchronize smoothly without overshoot or circulating current bursts.

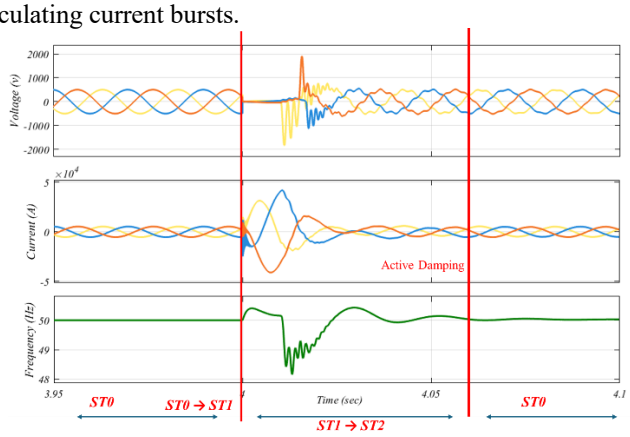

Figure 6. Fault response with static VI: high overcurrent peaks, weak damping, and large frequency oscillations during $ST_0 \rightarrow ST_1 \rightarrow ST_2$.

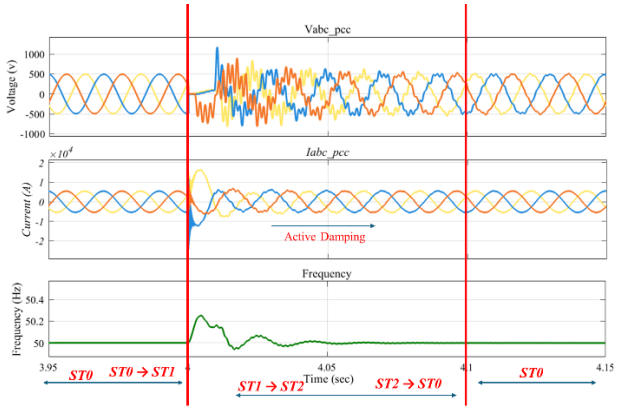

Figure 7. Fault response with proposed AVI: effective current limiting, fast post-fault damping, and smooth reconnection with suppressed inrush.

V. Conclusion

This paper presented a unified Multi-State AVI controller that enables reliable current limiting, fast post-fault recovery, and accurate power sharing in heterogeneous parallel GFMIs. By dynamically reconfiguring its R/X profile across ST_0–ST_2, the controller preserves GFM behaviour under faults, suppresses circulating currents, and provides strong transient damping without mode switching. Simulation results in MATLAB/Simulink verify significant improvements in stability, protection interoperability, and coordinated operation, demonstrating the suitability of the proposed approach for future inverter-dominated power systems.

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