Protection Hardware-in-the-Loop Validation for Inverter-Dominated Transmission Systems of Hawai'i Island

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***Abstract*—The increasing penetration of Inverter-Based Resources (IBRs) presents complex challenges to traditional grid protection, especially regarding the interplay between IBR overcurrent protection and overall system reliability. This paper introduces a real-time approach to developing and validating Control and Protection (C&P) functions for IBRs and their associated devices within the Hawaii Island transmission system, a grid rapidly transitioning to IBR-dominated generation. Our objective was to achieve protection reliability equivalent to existing schemes, targeting fault clearance within 5 cycles (83ms), defined by dependability, security, and fast fault clearance. Validation occurred in a real-time Protection Hardware-in-the-Loop (PHIL) testbed, uniquely marrying advanced inverter protection with established system protection schemes. This sophisticated environment integrated commercial Siemens SiProtec relays within a detailed Hawaiian Electric Company's transmission network model. Comprehensive testing covered balanced and unbalanced faults at critical locations. Key achievements included precise circuit breaker control using actual trip/block commands via real-time Generic Object Oriented Substation Events (GOOSE) messaging, and recloser logic for temporary/permanent faults.**

***Index Terms*—Inverter-Based Resources (IBRs), Control & Protection, Hardware-in-the-Loop (HIL), SiProtec Relays, Hawaiian Electric Company**

I. Introduction

The global energy landscape is undergoing a profound transformation, driven by the increasing integration of Inverter-Based Resources (IBRs) such as solar photovoltaics and wind power into electricity grids [1]. While IBRs offer significant environmental and economic benefits, their distinct operational characteristics, particularly during fault conditions, pose unprecedented challenges to the stability and reliability of power grids [2]. Unlike traditional synchronous generators that contribute high, predictable fault currents, IBRs often exhibit limited and controlled fault current contributions, which can desensitize conventional overcurrent and distance protection schemes [3]. This fundamental difference necessitates a re-evaluation and adaptation of existing Control and Protection (C&P) philosophies to ensure continued resilience and safety.

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Previous research has extensively explored various aspects of IBR fault behavior [4], the impact of low-inertia systems on protection coordination [5], and conceptual solutions for IBR-friendly protection algorithms. Studies have also investigated the challenges of conventional protection relays in grids with high IBR penetration through simulation [6]. Most recently, new studies have shown significant promise in this area of IBR-dominated protection coordination by comprehensive analysis of different fault conditions when subject to different protection schemes [7]. However, a significant research gap persists in the comprehensive, real-time validation of integrated IBR and system protection schemes [8]. Specifically, the complex and often unexplored interplay between IBR internal overcurrent protection strategies and the performance of commercial, off-the-shelf grid-level protection devices in a realistic grid context remains a critical area needing further investigation. The challenge is further compounded in grids with high IBR penetration, where the dynamic response of grid-forming (GFM) IBRs during faults can significantly influence protection operation and coordination.

Addressing this critical and timely need, this paper presents a real-time Protection Hardware-in-the-Loop (PHIL) approach to developing and rigorously validating advanced C&P functions for IBRs and their associated protection devices. Our work uniquely marries advanced inverter protection characteristics with established system protection schemes within a high-fidelity, real-time PHIL testbed, mainly focusing on PHIL implementation in a 100% renewable grid, and studying the interplay between inverter and system protection schemas. This research is specifically tailored for the Hawaiian Electric Company (HECO) Island transmission network, a grid rapidly transitioning towards IBR-dominated generation, making it an important case study for future-grid challenges and offering critical insights into IBR-grid integration. The primary objective was to achieve protection reliability equivalent to existing conventional schemes, specifically targeting fault clearance within an ambitious timeframe of 5 cycles (83ms), rigorously defined by dependability (correct operation during faults), security (non-operation under normal conditions), and consistently fast fault clearance. Unlike prior efforts, our methodology integrates commercial Siemens SiProtec protection devices directly into a detailed, real-time model of HECO,

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facilitating comprehensive testing under realistic operational scenarios and providing a robust platform for validating integrated protection performance for 64 distinct test cases, analyzing the system's performance under various balanced and unbalanced fault conditions.

II. Overview of System Models

A. Hawaii Island Transmission System Model

A real-time simulation model of HECO Island grid was developed for advanced fault response testing capabilities. A major development involved the successful implementation of updated simulation models on the OPAL-RT platform, with particular emphasis on Fault Ride-Through ($FRT\#1 - \#4$) functionalities [9]. These FRT capabilities have been comprehensively deployed and validated across four relevant network buses equipped with GFM IBRs within the Hawaiian Island power system model, as depicted in Fig. 1. This enables robust fault analysis to be conducted at each specified location.

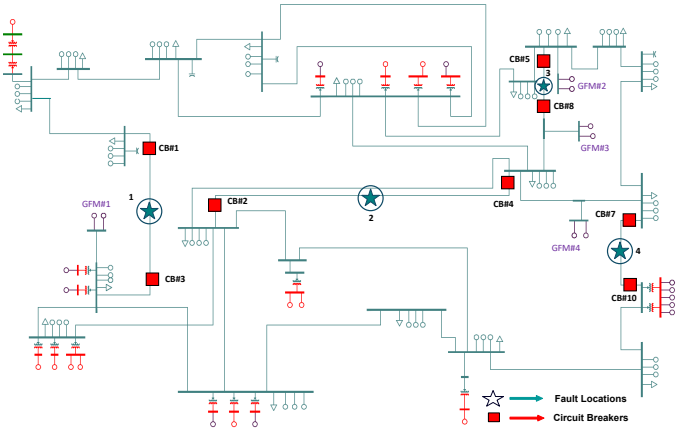

Fig. 1: Single line diagram (SLD) of the HECO test system, depicting the identified fault locations.

Fig. 1 illustrates the single line diagram of Hawaiian Island's extended power system, featuring a high penetration of non-synchronous generation. The model includes key GFM IBR locations such as two 50 MW solar-plus-50 MW battery systems near Kailua Kona (GFM#1) and Hualalai, and a 100 MW solar-plus-100 MW battery system near Hilo ($GFM\#2, \#3$). An additional 100 MW Battery Energy Storage System (BESS) is situated towards the southern part of the island (GFM#4). These interconnected resources form a comprehensive representation of the island's IBR dominated areas.

B. PHIL Testbed Architecture

The validation process is centered around a PHIL testbed. In this setup, commercial Siemens' SiProtec relays [10] are combined with a detailed, real-time simulation of the grid. Fig. 2 shows a zoomed-in view of the RT-LAB model, specifically focusing on a critical fault location (marked '1' in Fig. 1). The faults are applied at the middle of the PI-section lines connecting buses A and B. Communication between the model and the protection device is illustrated in the blue boxed areas. The real-time simulations are run in the OPAL-RT's OP5707XG real-time simulator [11]. The interface between Siemens SiProtec protection relays and the real-time simulation shown in Fig. 3, leverages standardized network protocols like IEC 61850 Sampled Measured Values (SMV) for the transmission of simulated grid measurements, and Generic Object Oriented Substation Events (GOOSE) for circuit breaker (CB) commands and status signals. This approach significantly simplifies the integration of relays when compared to the traditional analog current and potential transformer (CT/PT) based instrumentation. The adoption of SMV not only ensures high-fidelity, high-sampling rate data transfer but also fundamentally streamlines the hardware architecture, obviating the need for numerous analog-to-digital converters and significantly reducing system complexity.

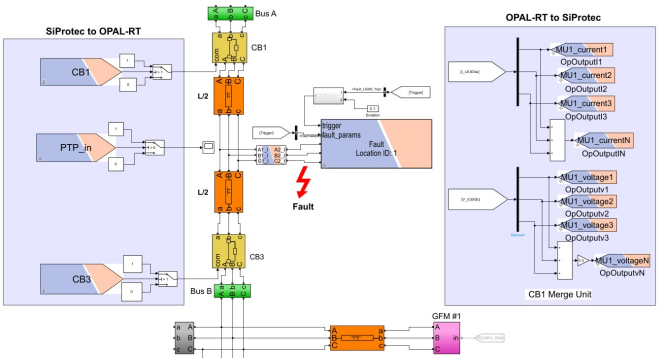

Fig. 2: Partial snippet of the HECO test system near GFM#1 inverter bus.

As a part of the PHIL testbed, a realistic substation configuration was developed with appropriate GOOSE communication configured between the OPAL-RT simulator and the SiProtec relays. The simulated SMV data streams, representing grid currents and voltages are transmitted between the OPAL-RT and SiProtec devices via virtual merging units instantiated inside the real-time simulator. Currently, four SiProtec relays are fully operational within the testbed, facilitating measurements at eight distinct locations (comprising four 3ϕ voltage measurements and eight 3ϕ current measurements). Extensive functional validation tests, encompassing various protection schemes, were successfully executed, confirming the efficacy of the integrated system.

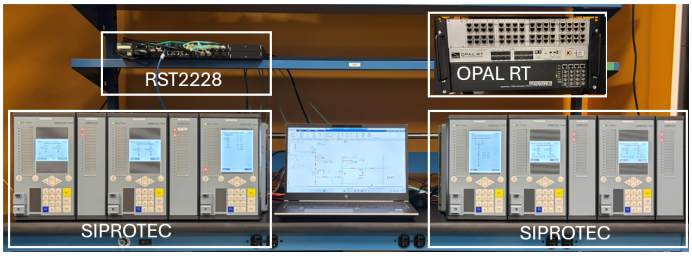

Fig. 3: PHIL testbed setup with SiProtec and OPAL-RT.

C. Protection Settings in SiProtec Relays

SiProtec $7SX85$ and $7SX82$ relays [10] are utilized for validating inverter protection in real-time, employing four different protection schemes. For overcurrent protection, pickup

currents are precisely set above the maximum load but below the minimum fault current (typically $1.2 - 1.5$ times the full-load current) to ensure reliable fault response without unnecessary tripping. Definite-time characteristics are implemented, featuring a Definite-T1 stage at 200 A for instantaneous clearance of high-current faults, and a Definite-T2 stage, also at 200 A but with a 0.3-second delay, for selective coordination and backup. All protection settings are applied to primary side values, as sampled mean values (SMVs) used to interface the relays. Distance protection, a primary scheme, measures line impedance to detect and isolate transmission line faults. With an equivalent line impedance of 31.75 Ω, the scheme is divided into three coordinated zones: Zone 1 covers 80% of the line (25.4 Ω) with instantaneous tripping, Zone 2 extends to 38 Ω with a 0.3-second delay for adjacent line backup, and Zone 3 provides remote backup at 47.625 Ω with a longer delay.

Complementing these, line current differential (LCD) protection enhances fault detection by comparing currents at both ends of a transmission line. This scheme is configured with an I-DIFF pickup of $230A$ for sensitivity to low differential currents, and an I-DIFF Fast 2 setting of $500A$ for rapid clearance of severe faults, ensuring both sensitive and high-speed responses. Further coordination is achieved through the permissive overreach transfer trip (POTT) mechanism. POTT coordinates tripping between relays at both line ends: each relay determines if a fault is within its overreaching Zone 2 and, if so, sends a permissive signal to the remote end. Tripping only occurs when both relays detect the fault within their respective overreaching zones and exchange permissive signals, guaranteeing secure and coordinated operation.

III. Results

A. Open Loop Real-time Performance

The "open-loop" nature of these tests mean, while the FRT function of the inverters are actively being tested in real-time under simulated fault conditions, the Siprotec relays, though monitoring, are not configured to communicate trip signals or any other feedback back into the system under this test. The main aim here is to assess the FRT behaviour while the fault is active on the system for 100 ms.

The inverter instantaneous currents for ABC-G fault near GFM inverter with FRT #3 activated is shown in Fig. 4. The first subplot shows a midline fault on fault location 1, whereas the second and third subplots show the inverter response when the fault is applied at 25% and 75% of the line length respectively for fault locations 2 and 3, as shown in Fig. 1. In all cases, the inverter is able to limit the current to 1.3 p.u. with the activation of FRT #3 during the fault after an initial spike for half cycle duration. Similarly, in Fig. 5, the inverter instantaneous currents for ABC-G fault near GFM inverter with FRT #4 activated is shown. FRTs limit over-current in symmetrical faults and actively contributes to system stability during by dynamically injecting both positive and negative sequence currents. The recovery of currents to their pre-fault values after fault clearance further confirms the effectiveness of the FRTs in the faulted scenarios.

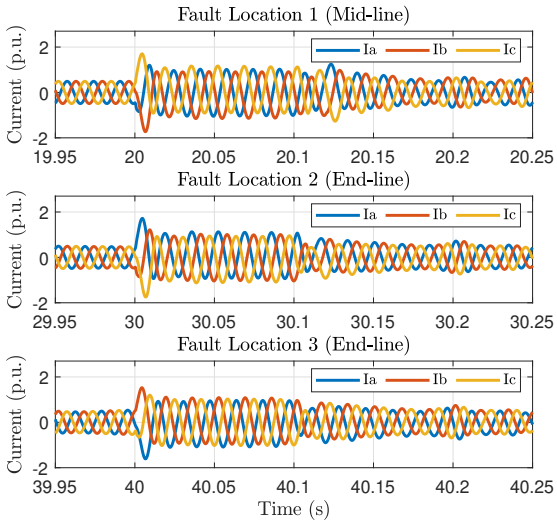

Fig. 4: 3ϕ current at inverter terminal for ABC-G fault with FRT3 activated.

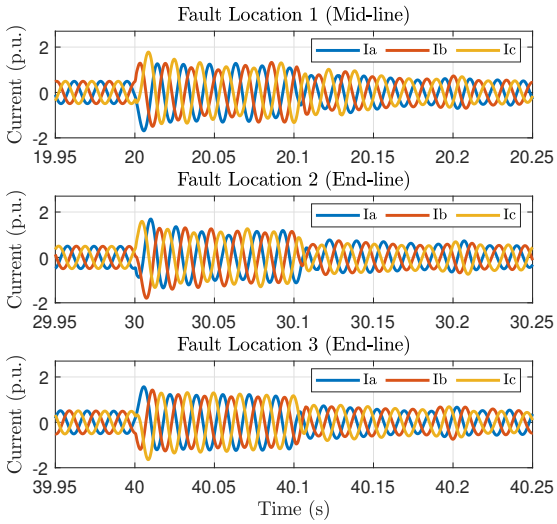

Fig. 5: 3ϕ current at inverter terminal for ABC-G fault with FRT4 activated.

B. Closed Loop Real-time Performance

Fig. 6 effectively illustrates the dynamic behavior of the three-phase currents (I_a, I_b, I_c) at the inverter terminal under various fault conditions (ABC-G, BC-G, A-G, and AB) within FRT #2 framework, specifically for distance protection. Each subplot clearly depicts the current waveforms before, during, and after a fault event. For the symmetrical ABC-G fault, all three phase currents exhibit a significant and balanced increase in magnitude and distortion during the fault, returning to their steady-state once the fault clears. In contrast, asymmetrical faults such as BC-G, A-G, and AB show distinct current responses: the faulted phases experience substantial increases and distortions, while unfaulted phases are either less affected or show altered patterns to maintain system balance. These plots collectively demonstrate the inverter's current contribution and the system's transient response to different fault types, which is crucial for evaluating the effectiveness of distance

protection schemes under FRT 2.

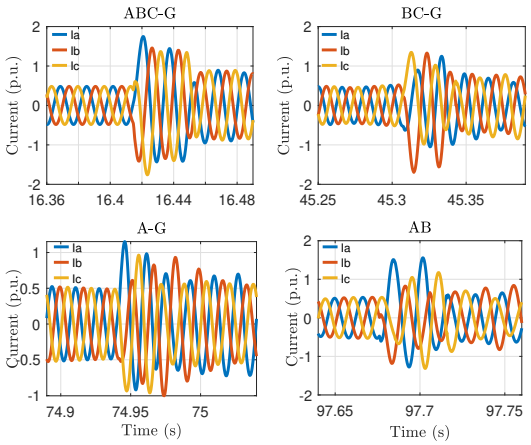

Fig. 6: 3ϕ current across inverter terminal with FRT2 for all types of faults for distance protection.

Fig. 7, and Fig. 8 illustrate the $FRT\#3$ and $FRT\#4$ functionality with line current differential and POTT protection schemes, respectively. These plots demonstrate the interplay between grid-side protection schemes and the inverter's inherent FRT overcurrent control. Upon fault initiation, each scenario consistently shows a rapid surge in inverter current, often peaking between 1 and 1.5 per unit, a key observation is the active role of the inverter's FRT overcurrent control and rapid interruption of faults by all protection schemes used for validation.

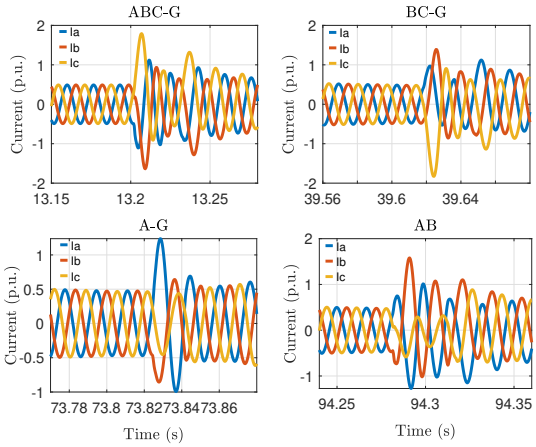

Fig. 7: 3ϕ current across inverter terminal with FRT3 for all types of faults for LCD protection.

Fig. 9 effectively demonstrates the performance of both Line Current Differential (LCD) protection in FRT #3 and POTT protection in FRT #4 across various fault conditions, by showcasing CB currents and their corresponding tripping times. For LCD protection, a three-phase-to-ground (ABC-G) fault (Case I) resulted in rapid, simultaneous tripping of both CB 1 and CB 3 in 15.4 ms, and 15.8 ms, respectively, while a phase-to-phase-to-ground (BC-G) fault (Case II) saw CB 1 trip in 14.5 ms and CB 3 in 13.3 ms, highlighting the scheme's quick and coordinated response. POTT protection, on the other hand, handled a single-phase-to-ground (A-G) fault (Case III)

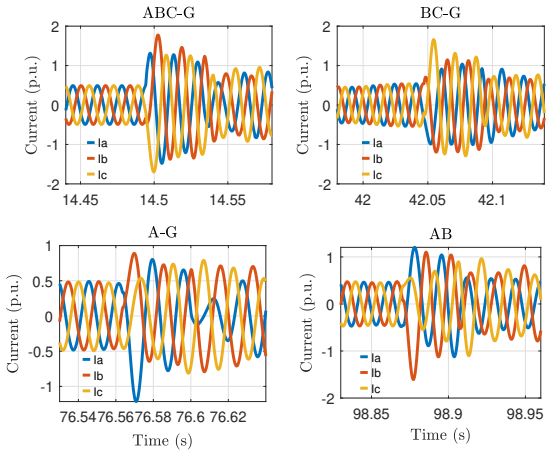

Fig. 8: 3ϕ current across inverter terminal with FRT4 for all types of faults for POTT protection.

with CB 1 tripping in 26.6 ms and CB 3 in 34 ms, and a phase-to-phase (AB) fault (Case IV) with CB 1 tripping in 30.4 ms and CB 3 in 30.7 ms, indicating effective, albeit slightly longer, coordinated tripping. In summary, the results confirm that both LCD and POTT protection schemes are successful in promptly detecting and isolating faults, with tripping times consistently within acceptable limits for maintaining system stability and reliability. Tables I, and II show clearing times

TABLE I: Clearing times (in ms) for all kinds of faults subject to FRT1 and FRT2 and four protection schemes.

		FRT1				FRT2			
		OC	Z	LCD	POTT	OC	Z	LCD	POTT
CB1	ABC-G	21	32.2	16.7	31.3	16.7	28.9	16.5	32.7
	BC-G	16.2	36.2	17.4	35.4	10	35.6	15.6	33.8
	A-G	16.5	37.3	20.2	26.6	14.4	24.5	18.2	26.7
	AB	20	34.9	17	35.1	20.04	34.1	16	30.4
CB3	ABC-G	14.3	30.8	17	34.9	14.1	32.7	16.9	40.9
	BC-G	18.9	24.2	18	38.6	10	23.5	15.7	41.3
	A-G	17.3	25.3	20.5	29.7	18.6	22.5	17.7	34.1
	AB	14	27.4	17	35.1	12	27	17	30.7

for all faults for a midline fault simulated at fault location 1, as shown in Fig. 1. CB 1 and CB 3 are the trip/block signals being received from SiProtec and acting on the circuit breakers in the real-time model. For all kinds of faults for all protection schemes, the fault clearing time is achieved in < 5 cycles.

TABLE II: Clearing times (in ms) for all kinds of faults subject to FRT3 and FRT4 and four protection schemes.

		FRT3				FRT4			
		OC	Z	LCD	POTT	OC	Z	LCD	POTT
CB1	ABC-G	20.2	37.9	15.4	28.3	19.6	33.2	14.9	32.7
	BC-G	21.1	25	14.5	28.9	16.7	33.4	18.7	33.9
	A-G	15.3	26.3	16.3	33.6	14.4	44.5	20.1	26.6
	AB	18.6	33.2	23.2	41	18.1	36.5	19.3	30.4
CB3	ABC-G	15.5	22.1	15.8	31.1	12.4	20.6	14.7	39.9
	BC-G	18.9	24.3	13.3	36	15.5	21	19.1	41.4
	A-G	14	20.7	16.2	36.6	15.6	31.1	20.03	34
	AB	13.7	31.9	23	42	12.4	28.1	19.5	30.7

IV. Conclusions and Future Directions

This paper successfully validates novel C&P functions tailored for IBRs and their associated protection devices within a high-fidelity, real-time Protection Hardware-in-the-Loop (PHIL) testbed. The results demonstrate that the newly

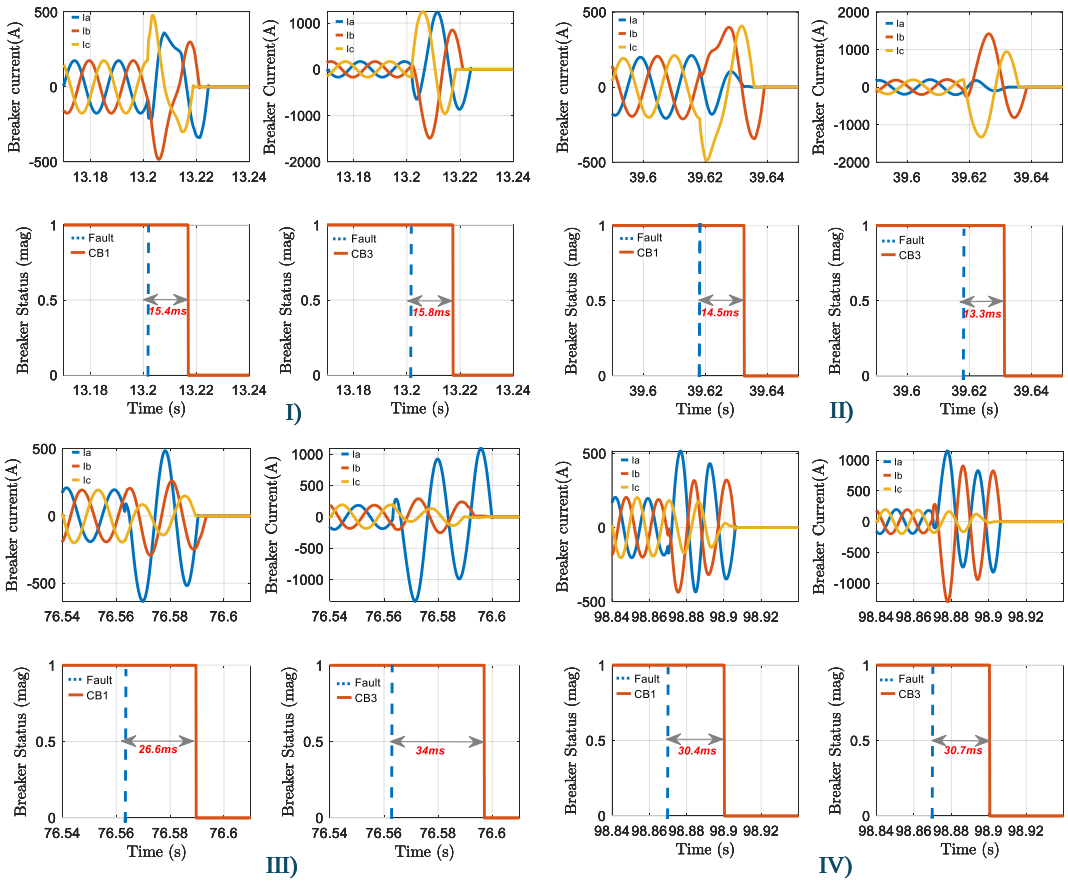

Fig. 9: CB current and status for LCD protection in FRT3 for faults I) ABC-G, II) BC-G and POTT protection in FRT4 for faults III) A-G, IV)AB.

developed C&P functions meet, and in some aspects surpass, the demanding protection reliability requirements for the Hawaii Island power system. Specifically, the system exhibited high dependability, ensuring reliable operation during fault conditions. Most importantly, all tested transmission line faults were consistently cleared well within 5-cycle (83 ms) timeframe. This comprehensive PHIL testbed validation, leveraging commercial-grade protection hardware within a real-time simulation environment, provides strong evidence for the practical efficacy and robustness of these advanced protection schemes for IBR-dominated power grids. Future work will focus on expanding the scope of testing to encompass a wider range of fault locations across the entire Hawaii Island system model, as well as evaluating performance under diverse operational scenarios, such as varying levels of IBR penetration and grid strength, and a mix of GFL and GFM inverter scenarios.

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