Phasor-Domain MMC Blocking Behavior Modeling

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***Abstract*—This paper proposes an improved phasor-domain model of the Modular Multilevel Converter (MMC) that incorporates arm-blocking behavior suitable for dynamic simulations. The model is based on an arm average-value model (AAVM) that includes the effect of antiparallel diodes through eleven ideal switches and three diodes that dynamically reconfigure the arm topology upon receiving a blocking signal. In normal operation, the switching states emulate the simplified AAVM. Meanwhile, in blocking mode, they switch back to emulate the conduction of the arm current through the anti-parallel diodes. To achieve this, equations for the blocking mode were derived with the goal of preserving the average internal dynamics of the converter. The proposed model is implemented in Modelica and simulated in Dymola, which effectively demonstrates blocking characteristics with minimal computational burden, making it well-suited for power system dynamic studies.**

***Index Terms*—Arm average-value model, MMC blocking, Modular multilevel converter (MMC), phasor approximation**

I. Introduction

The increasing complexity of power systems, driven by renewable integration and long-distance energy transfer, has position High Voltage Direct Current (HVDC) systems as a key enabler of future transmission networks. Among the available topologies, the Modular Multilevel Converter (MMC) has become the preferred choice for HVDC systems due to its modularity, scalability, and ability to produce high-quality voltage waveforms [1], [2]. Although electromagnetic transient (EMT) models of MMCs provide the most accurate representation of MMCs, they can be computationally demanding when dealing with large-scale and/or complex AC/DC networks. Alternatively, phasor-domain models are able to capture essential converter behavior while significantly improving simulation speed. Arm average-value model (AAVM), in particular, has been shown to enable faster simulations with reduced complexity [1], [2]. These models approximate MMC dynamics by balanced submodule capacitor voltages in each arm.

Conventional AAVMs models do not account for blocking operation, an important protective mode activated during faults, in which all IGBT switches of each MMC submodule are turned off simultaneously and current is redirected through anti-parallel diodes [3], [4], [5]. This limits the application of existing AAVM models, in particular, to gain insight on AC/DC dynamics under faults or during post-fault recovery. Although there are EMT models capable of blocking [4], they are computationally demanding [6]. Recent AAVM extensions have incorporated blocking through thyristor-based switching, However, its application remains limited to a single simulation tool, lacks generalization for implementation across simulation environments or applicability to large-system simulation [3]. Similarly, an EMT-compatible switching model that captures the behavior of MMC on the half- and full-bridge during blocking is presented in [4], but it was not adapted for its use in phasor-domain simulation frameworks.

This paper proposes a generalized phasor-domain MMC model that incorporates arm-blocking behavior through 11 ideal switches and three diodes. The model preserves the averaged internal dynamics in both blocked and deblocked modes. The model is implemented in the Modelica language and integrated with the OpenIPSL library [7]. The simulation results confirm the expected blocking behavior.

The remainder of the paper is organized as follows. Section II reviews the conventional AAVM. Section III develops the proposed blocking-capable model. Section IV discusses simulation results. Section V concludes the paper.

II. Conventional AAVM MMC Model

The detailed model (DM) of the three-phase MMC topology is illustrated in Fig. 1a. Each phase consists of an upper and a lower arm, where each arm comprises a series connection of identical submodules (SMs), an arm resistance, R_{arm}, and an arm inductance, L_{arm}. Each SM is a half-bridge converter composed of two IGBTs, V_{T1}, and V_{T2} and a capacitor, C, as shown in Fig. 1b. For a sufficiently large number of SMs, and when the focus is on ac and dc current dynamics under appropriate energy-based control [2], [8], [9], the average voltages of all SM capacitors in an arm remain nearly equal. Hence, all SM capacitors can be represented by a single equivalent capacitor, $C_{tot_{arm}} = C/N$, where C is the capacitance of the SM and N is the number of SMs per arm. Each arm of the MMC can then be modeled as a controlled voltage source, as illustrated in Fig. 1c, regulated by a coupling loop consisting of a controlled current source and an equivalent arm capacitor [10]. The AAVM is thus derived, as depicted in Fig. 2a. Since the power imbalance between the ac and dc sides of the converter is generally negligible [1], the control system maintains a voltage equilibrium between the upper and lower arms such that $(v_{C_{tot_{uj}}})^2 - (v_{C_{tot_{lj}}})^2 = 0$. Hence,

$$v_{C_{tot_{uj}}} \approx v_{C_{tot_{lj}}} = \bar{v}_{C_{tot_j}} = \frac{v_{C_{tot_{uj}}} + v_{C_{tot_{lj}}}}{2} \tag{1}$$

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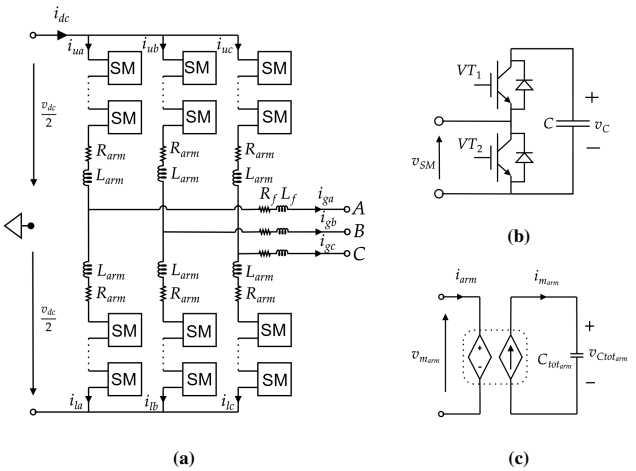


(a) (b) (c)

Fig. 1: (a) MMC detailed model. (b) Submodule. (c) Equivalent arm model.

In (1), $v_{C_{tot_{uj}}}$ and $v_{C_{tot_{lj}}}$ are the total equivalent capacitor voltages of the upper and lower arms of phase j, while $\bar{v}_{C_{tot_j}}$ represents their average. The total stored energy in the converter is assumed to be equally shared between all phases [2], giving the following.

$$\bar{v}_{C_{tot_a}} = \bar{v}_{C_{tot_b}} = \bar{v}_{C_{tot_c}} = \bar{v}_{C_{tot}}. \tag{2}$$

Taking into account the assumptions in (1) and (2), the phasor-domain AAVM of the MMC is derived as shown in Fig. 2b, and its dynamic behavior can be expressed by the following equations:

$$v_{md} - v_{gd} = L_{eq}^{ac}\frac{di_{gd}}{dt} + R_{eq}^{ac}i_{gd} - \omega L_{eq}^{ac}i_{gq} \tag{3}$$

$$v_{mq} - v_{gq} = L_{eq}^{ac}\frac{di_{gq}}{dt} + R_{eq}^{ac}i_{gq} + \omega L_{eq}^{ac}i_{gd} \tag{4}$$

$$v_{dc} - v_{mdc} = L_{eq}^{dc}\frac{di_{dc}}{dt} + R_{eq}^{dc}i_{dc} \tag{5}$$

$$C_{eq}\frac{d\bar{v}_{C_{tot}}}{dt} = m_{dc}i_{dc} - m_d i_{gd} - m_q i_{gq} \tag{6}$$

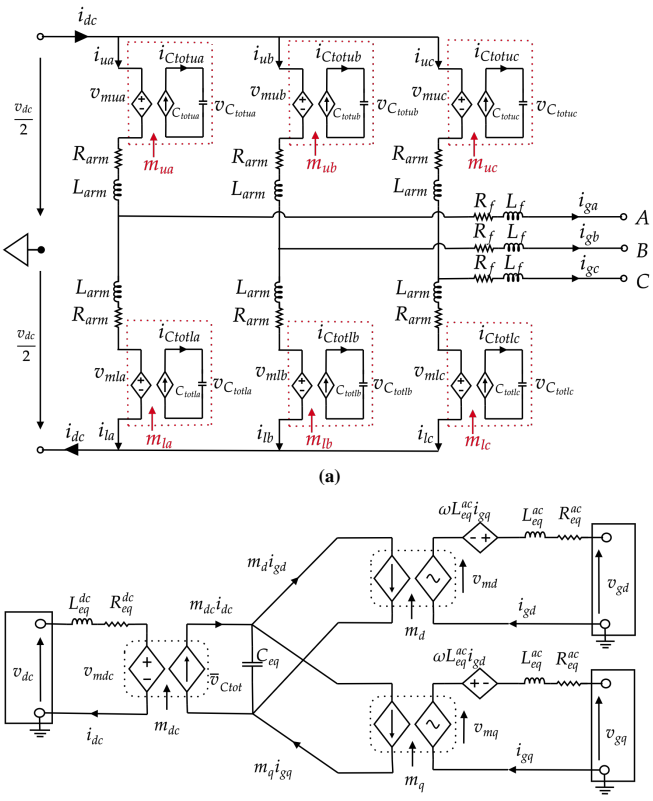
where

$$m_d = \frac{v_{md}}{\bar{v}_{C_{tot}}}, \quad m_q = \frac{v_{mq}}{\bar{v}_{C_{tot}}}, \quad m_{dc} = \frac{v_{mdc}}{\bar{v}_{C_{tot}}} \tag{7}$$

$$R_{eq}^{dc} = \frac{2R_{\text{arm}}}{3}, \quad L_{eq}^{dc} = \frac{2L_{\text{arm}}}{3} \tag{8}$$

$$R_{eq}^{ac} = \frac{R_{arm} + 2R_f}{2}, \quad L_{eq}^{ac} = \frac{L_{arm} + 2L_f}{2} \tag{9}$$

The modulated voltages v_{md}, v_{mq}, and v_{mdc} serve as control inputs that regulate the dynamics of the converter, along with the corresponding grid voltages v_{gd} and v_{gq}. Meanwhile, i_{gd} and i_{gq} represent the current components of the grid on the d- and q-axes, and ω is the frequency of the ac system. The average voltage of the arm-capacitor is $\bar{v}_{C_{tot}}$, with an equivalent capacitance $C_{eq} = 6C_{tot}$. The modulation indices are m_d, m_q, and m_{dc}. The equivalent ac parameters are R_{eq}^{ac} and L_{eq}^{ac}, while the dc parameters are R_{eq}^{dc} and L_{eq}^{dc}, where R_{arm}, L_{arm}, R_f, and L_f denote the resistances and inductances of the arm and transformer.



(a)

(b)

Fig. 2: (a) Conventional AAVM. (b) MMC phasor model.

III. Proposed Blocking Capability Modeling

When the MMC enters blocking mode, all IGBT switches in SMs are turned off simultaneously. Due to the anti-parallel diodes, the arm current (i_{arm}) cannot drop to zero instantaneously [3]–[5]. Depending on its direction, the SM capacitors are either charged or bypassed. For a positive arm current, as shown in Fig. 3a, the current flows through the upper diodes until it decays to zero, charging the SM capacitors. To reproduce this behavior, the equivalent arm model in Fig. 1c is modified, as illustrated in Fig. 3c, where four switches are added. During blocking, SW_1 and SW_2 are ON while SW_4 and SW_5 are OFF; the reverse applies in normal operation. For a negative arm current, as shown in Fig. 3b, the current flows through the lower diodes until it reaches zero, bypassing the SM capacitors and charging the dc side. The corresponding equivalent arm model is shown in Fig. 3d, it uses three switches. Here, SW_3 is ON while SW_4 and SW_5 are OFF during blocking. The resistances to the ON and the OFF-state are given by [4]:

$$R_{ON} = \frac{R_{I_{OFF}} \cdot R_{D_{ON}}}{R_{I_{OFF}} + R_{D_{ON}}}, R_{OFF} = \frac{R_{I_{OFF}} \cdot R_{D_{OFF}}}{R_{I_{OFF}} + R_{D_{OFF}}} \tag{10}$$

where $R_{I_{OFF}}$, $R_{D_{ON}}$, and $R_{D_{OFF}}$ are the resistances of the IGBT (OFF-state), diode (ON-state), and diode (reverse-biased), respectively.

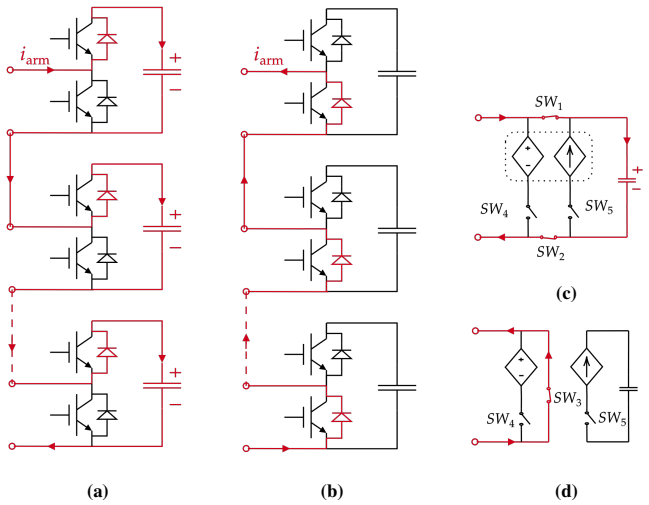


Fig. 3: Direction of the arm current flow: (a) Positive, (b) Negative; Arm equivalent models for: (a) Positive arm current, (b) Negative arm current.

A. Blocking Model Development for Positive Arm Current

The structure of the blocking strategy adopted for each arm for the positive arm current is imposed on the AAVM model shown in Fig. 4a. Arm currents i_{uj} (i_{lj}) flow directly through the arm capacitors. Hence, the capacitor currents are given by

$$i_{uj} = i_{C_{tot_{uj}}} = C_{tot}\frac{dv_{C_{tot_{uj}}}}{dt};\;\; i_{lj} = i_{C_{tot_{lj}}} = C_{tot}\frac{dv_{C_{tot_{lj}}}}{dt} \tag{11}$$

Applying KVL and KCL in phase j, yields

$$\frac{V_{dc}}{2} - v_{C_{tot_{uj}}} - L_{arm}\frac{di_{uj}}{dt} - R_{arm}i_{uj} - L_f\frac{di_{gj}}{dt} - R_f i_{gj} - v_{gj} = 0 \tag{12}$$

$$-\frac{V_{dc}}{2} + v_{C_{tot_{lj}}} + L_{arm}\frac{di_{lj}}{dt} + R_{arm}i_{lj} - L_f\frac{di_{gj}}{dt} - R_f i_{gj} - v_{gj} = 0 \tag{13}$$

Taking into account (8) and (9), the addition and subtraction of (12) and (13) yield the following

$$v_{vj_+} - v_{gj} = L_{eq}^{ac}\frac{di_{gj}}{dt} + R_{eq}^{ac}i_{gj} \tag{14}$$

$$v_{dc} - v_{diff_{j+}} = 2L_{arm}\frac{di_{diff_j}}{dt} + 2R_{arm}i_{diff_j} \tag{15}$$

where

$$i_{gj} = i_{uj} - i_{lj} \tag{16}$$

$$v_{vj_+} = \frac{-v_{C_{tot_{uj}}} + v_{C_{tot_{lj}}}}{2} \tag{17}$$

$$i_{diff_j} = \frac{i_{uj} + i_{lj}}{2} \tag{18}$$

$$v_{diff_{j+}} = v_{C_{tot_{uj}}} + v_{C_{tot_{lj}}} \tag{19}$$

Taking into account (1) in (17) and (19) yields:

$$v_{vj_+} = 0, \quad v_{diff_{j+}} = 2\bar{v}_{C_{tot_j}} \tag{20}$$

As a result, (14) and (15) becomes:

$$-v_{gj} = L_{eq}^{ac}\frac{di_{gj}}{dt} + R_{eq}^{ac}i_{gj} \tag{21}$$

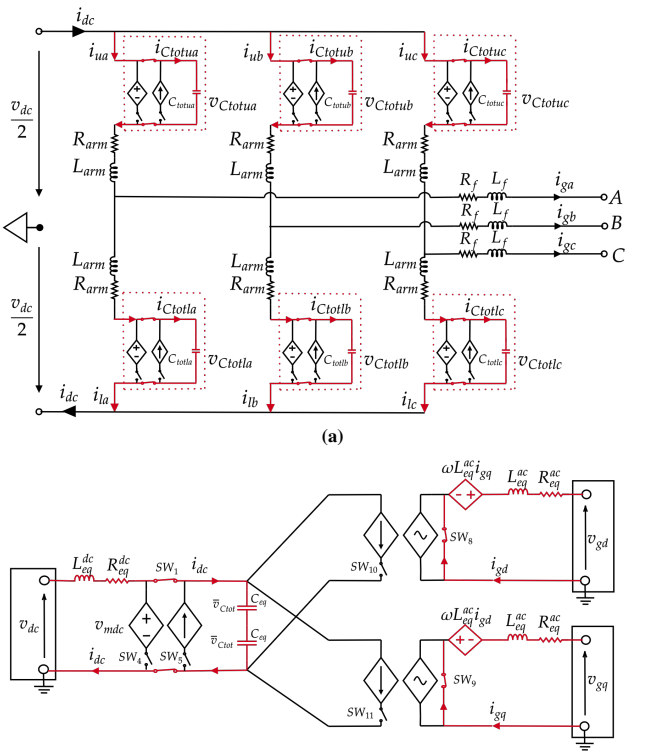


Fig. 4: Blocking model for positive arm current: (a) Conventional AAVM, (b) Phasor model.

$$V_{dc} - 2\bar{v}_{C_{tot_j}} = 2L_{arm}\frac{di_{diff_j}}{dt} + 2R_{arm}i_{diff_j} \tag{22}$$

The combination of (1), (11) and (18), and the addition of upper and lower arm capacitor currents, gives:

$$2C_{tot}\frac{d\bar{v}_{C_{tot_j}}}{dt} = i_{uj} + i_{lj} = 2i_{diff_j} \tag{23}$$

Taking into account $\sum(i_{diff_j}) = i_{dc}$, and $C_{eq} = 6C_{\text{tot}}$, summing (23) over three phases yields:

$$C_{eq}\frac{d\bar{v}_{C_{totj}}}{dt} = 2i_{dc} \tag{24}$$

Furthermore, the ac dynamics in (21) can be decomposed into:

$$-v_{gd} = L_{eq}^{ac}\frac{di_{gd}}{dt} + R_{eq}^{ac}i_{gd} - \omega L_{eq}^{ac}i_{gq} \tag{25}$$

$$-v_{gq} = L_{eq}^{ac}\frac{di_{gq}}{dt} + R_{eq}^{ac}i_{gq} + \omega L_{eq}^{ac}i_{gd} \tag{26}$$

Finally, the dc dynamics in (22) is simplified as:

$$V_{dc} - 2\bar{v}_{C_{tot}} = L_{eq}^{dc}\frac{di_{dc}}{dt} + R_{eq}^{dc}i_{dc} \tag{27}$$

The final equivalent circuit in the phasor domain of blocking mode MMC for positive arm current is shown in Fig. 4b.

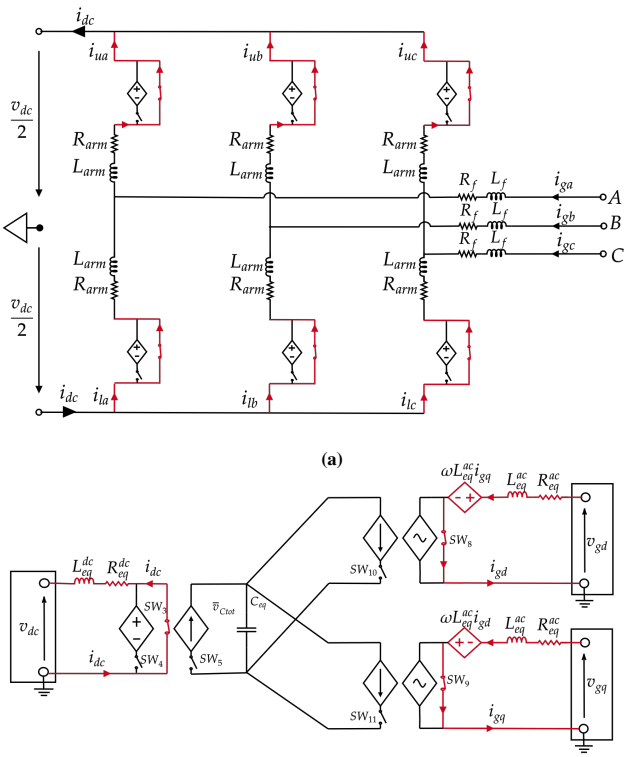


Fig. 5: Blocking model for negative arm current: (a) Conventional AAVM. (b) Phasor model.

B. Blocking Model Development for Negative Arm Current

The AAVM model in Fig. 5a incorporates the blocking scheme for the negative arm current. Arm currents i_{uj} (i_{lj}) bypass arm capacitors. Applying KVL and KCL in phase j gives

$$-\frac{V_{dc}}{2} - L_{arm}\frac{di_{uj}}{dt} - R_{arm}i_{uj} - L_f\frac{di_{gj}}{dt} - R_f i_{gj} + v_{gj} = 0 \quad (28)$$

$$\frac{V_{dc}}{2} + L_{arm}\frac{di_{lj}}{dt} + R_{arm}i_{lj} - L_f\frac{di_{gj}}{dt} - R_f i_{gj} + v_{gj} = 0 \quad (29)$$

Taking into account (8) and (9), the addition and subtraction of (28) and (29) yields

$$v_{gj} = L_{eq}^{ac}\frac{di_{gj}}{dt} + R_{eq}^{ac}i_{gj} \quad (30)$$

$$-V_{dc} = 2L_{arm}\frac{di_{diff_j}}{dt} + 2R_{arm}i_{diff_j} \quad (31)$$

where

$$i_{gj} = i_{uj} - i_{lj} \quad i_{diff_j} = \frac{i_{uj} + i_{lj}}{2} \quad (32)$$

The ac dynamics in (30) can be decomposed as follows

$$v_{gd} = L_{eq}^{ac}\frac{di_{gd}}{dt} + R_{eq}^{ac}i_{gd} - \omega L_{eq}^{ac}i_{gq} \quad (33)$$

$$v_{gq} = L_{eq}^{ac}\frac{di_{gq}}{dt} + R_{eq}^{ac}i_{gq} + \omega L_{eq}^{ac}i_{gd} \quad (34)$$

Given $\sum(i_{diff_j}) = i_{dc}$, the dc dynamics in (32) become

$$-V_{dc} = L_{eq}^{dc}\frac{di_{dc}}{dt} + R_{eq}^{ac}i_{dc} \quad (35)$$

The final equivalent circuit is shown in Fig. 5b.

C. Combination of Both Positive and Negative Arm Current

Figure 6 shows the complete phasor domain AAVM model with blocking capability by combining the positive arm current equivalent circuit in Fig. 4(b) and the negative arm current equivalent circuit in Fig. 5(b). Eleven switches and three diodes propose blocking. In normal operation, switches 1, 2, 3, 7, 8 and 9 are OFF and 4, 5, 6, 10 and 11 are ON while all the diodes are in reverse bias. When blocking occurs, switches 1, 2, 3, 7, 8, and 9 are ON and 4, 5, 6, 10 and 11 are OFF. For the positive arm current, diodes 1 and 2 conduct while diode 3 does not, charging the equivalent capacitor. For the negative arm current, diodes 1 and 2 are non-conducting and diode 3 is conducting, bypassing the corresponding capacitor.

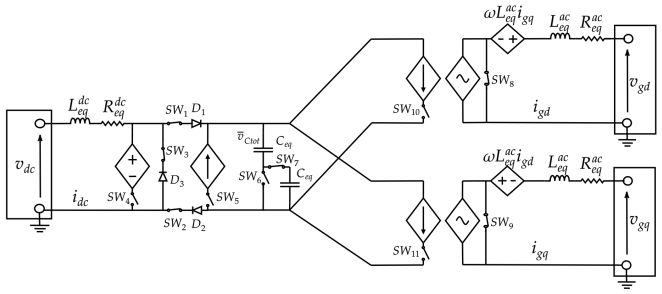


Fig. 6: Phasor Domain MMC model with blocking capability

IV. Simulation Studies

The proposed phasor-domain AAVM-based MMC model with blocking capability is implemented using the Modelica language. For simulation, Dymola efficiently handles hybrid systems by combining continuous electrical dynamics with discrete switching events [11], making it suitable for modeling converter blocking [12]. Ideal switches and diodes governed by logical conditions represent both operating modes, while the structure follows OpenIPSL-style modularity for compatibility with large-scale phasor-domain ac/dc studies [7].

The single MMC is connected to a simplified AC grid, as shown in Fig. 7, is used to validate the model proposed in Fig. 6. On the ac side it includes an ac source v_{ac} and a transformer T_N. On the dc side it includes a dc source V_{dc} with a series resistor R_{dc} and the proposed converter operating under P–Q control. The switches and diodes used to replicate

TABLE I: Simulation Parameters of the System

Quantity	Parameter	Value
AC System	AC voltage (v_{ac})	320 kV
	Base frequency (f_b)	50 Hz
Transformer	Transformer inductance (L_f)	0.18 p.u.
	Transformer resistance (R_f)	0.001 p.u.
MMC	Arm inductance (L_{arm})	0.0758 p.u.
	Arm resistance (R_{arm})	0.0078 p.u.
	Number of submodules per arm (N_{arm})	200
	SM capacitance (C_{sub})	10 mF
	Rated power (MVA_b)	1000 MVA
DC System	DC voltage (V_{dc})	640 kV
	DC resistance (R_{dc})	10 Ω

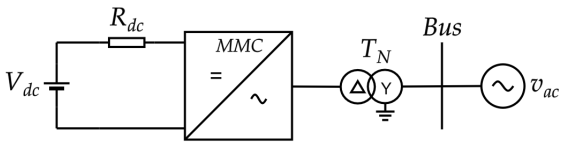


Fig. 7: Simulation system of single MMC interfaced to a ac grid.

the blocking modes are modeled as ideal elements, with an OFF-state resistance of 1 MΩ and an ON-state resistance of 0.1 mΩ. The system parameters are listed in Table I.

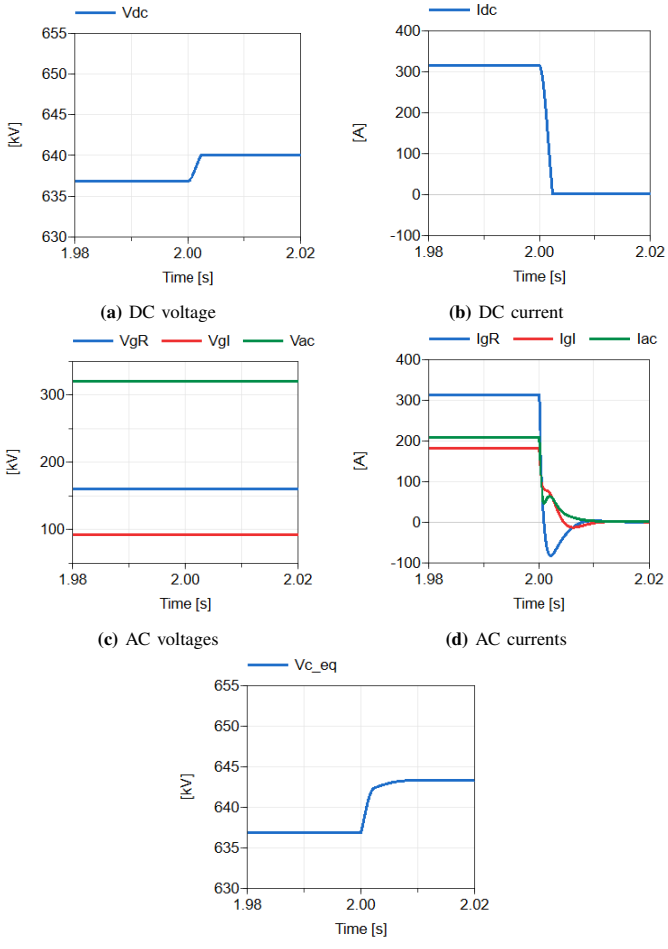
The converter operates in the normal state in the P-Q control mode with an active power reference of 0.2 p.u. and a reactive power reference of 0 p.u. A block signal is applied to the MMC at $t = 2$ s. The resulting waveforms during the interval $t = 1.98$ s to $t = 2.02$ s are shown in Fig. 8.

The voltage and current on the dc side of the MMC are shown in Fig. 8a and Fig. 8b, respectively. After applying the blocking signal at $t = 2$ s, the dc voltage increases and settles to a steady value while the dc current gradually decreases to zero, as expected when the converter stops transferring active power.

The voltage and current on the ac side of the MMC are shown in Fig. 8c and Fig. 8d, respectively. The ac voltage remains undisturbed while the AC current starts to decay after blocking and reaches zero in approximately 15 ms. This transition occurs as the arm current is redirected through antiparallel diodes.

The equivalent capacitor voltage of the MMC is shown in Fig. 8e. A small voltage rise is observed following blocking, caused by the anti-parallel diode conduction from residual positive current in the arms charging the capacitors. Once the transient subsides, the voltage remains constant.

These results closely match the simulation behavior reported in [3], where a blocking-capable AAVM produced nearly identical current extinction and capacitor charging dynamics, reinforcing the validity of the proposed model.



(a) DC voltage **(b)** DC current

(c) AC voltages **(d)** AC currents

(e) Capacitor voltage

Fig. 8: Simulation results of the proposed MMC blocking model.

V. Conclusion

In this work a phasor-domain MMC model was derived from a simplified Arm Average-Value Model that is capable of simulating arm-blocking behavior with minimal computational complexity. The model demonstrates blocking within the simplified AAVM framework utilizing eleven switches and three diodes. The implementation in Modelica and the simulation in Dymola shows the expected behavior and prove that the model can mimic blocking conditions. Future research will focus on validating the simplified model against EMT simulation to assess its fidelity across various operating scenarios, as well as quantifying accuracy limits and expanding its applicability to assess limitations under unbalanced fault conditions and other AC/DC system simulation needs.

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