Analysis of DC Voltage Ripple in Grid-Connected Inverters under Unbalanced Disturbances in Weak Grids

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***Abstract*-- Voltage unbalance in the power grid can cause twice-frequency ripple in the DC capacitor voltage of grid-connected inverters, which affects their lifespan and control performance. In weak grid conditions, the dynamic interaction between the inverter and the grid is intensified, leading to deviations in traditional calculations for DC voltage ripple, potentially resulting in improper DC capacitor design. To address this, a small-signal model is developed by analyzing the propagation path of unbalanced disturbances between the inverter and the weak grid. This model accurately quantifies both the transient and steady-state ripple magnitudes of the capacitor voltage following unbalanced disturbances. Additionally, constraint surfaces for capacitor values under transient/steady-state ripple limits are calculated. Finally, Controller-hardware-in-the-loop experiments validate the accuracy of the proposed model. The findings provide clear boundary conditions for DC capacitor design, enhancing the safety and reliability of inverter grid-connected operations.**

***Index Terms*—Unbalanced Disturbances; Weak AC grid; Grid-Connected Inverters; DC-link Capacitor**

I. Introduction

With the widespread integration of single-phase loads such as electric vehicles and new energy storage systems, the voltage unbalance in distribution networks is gradually increasing. When the distribution network operates under unbalanced conditions, twice-frequency ripple in the active power on the AC side leads to corresponding twice-frequency ripple in the inverter's DC-link capacitor voltage, which severely impacts the control performance of the grid-connected system [1]. Typically, voltage ripple at twice-frequency can be suppressed by using a larger DC-link capacitor. However, over-sizing the DC-link capacitor increases the inverter's volume and cost, while under-sizing it can worsen the voltage ripple, increase the operational temperature, and subject the capacitor to higher dielectric voltage stress, severely affecting its lifespan [2]. Therefore, accurately quantifying the transient and steady state twice-frequency ripple sizes following unbalanced disturbances and defining the boundary constraints for DC-link capacitor sizing are essential for the economical and reliable operation of grid-connected inverters.

Currently, most studies calculate the steady-state value of twice-frequency voltage ripple under unbalanced operation using power balance equations, while research on the quantification of transient ripple caused by unbalanced disturbances is relatively scarce. References [3], [4], [5] use the symmetrical component method to derive expressions for the sequence components of DC voltage ripple in inverters with unbalanced loads. References [6] established a transfer function considering the grid-connected line and grid impedance, while ignoring the dynamics of the inverter control loop, to calculate the DC voltage gain caused by unbalanced disturbances. Reference [7] analyzes the DC-link voltage oscillations in grid-connected inverters caused by harmonic current injection for active filtering. Reference [8] analyzes the low-frequency DC-link current and voltage ripple in multiphase voltage source inverters under unbalanced load conditions using symmetrical sequence components and energy balance principles. However, these methods focuses primarily on steady-state ripple quantification and does not account for the transient dynamics or the closed-loop interactions between the inverter control system and grid impedance during disturbances. Reference [9] develops a dynamic phasor model to analyze the transient response of inverter-based microgrids under unbalanced conditions. However, it does not specifically address the DC voltage ripple constraints for capacitor design under weak grid conditions. As the strength of the AC grid weakens, the interaction between the weak grid and the inverter control loop intensifies. The voltage ripple continuously affects the inverter's terminal voltage through the modulation loop, and the dynamics of the phase-locked loop under unbalanced input, among other factors, cause the system to remain in a weak dynamic state near the stable point, rather than transitioning from transient to steady-state. This results in deviations in traditional steady-state voltage twice-frequency ripple calculations, which may lead to improper capacitor sizing. Furthermore, as the equivalent impedance of the AC grid increases, the transient voltage ripple caused by unbalanced disturbances becomes increasingly significant. Relying solely on steady-state ripple constraints to design the capacitor size may fail to meet the voltage ripple requirements during transient processes.

To address this, this paper first analyzes the limitations of traditional voltage twice-frequency ripple calculation methods under weak grid conditions. Then, by analyzing the propagation path of unbalanced disturbances between the inverter and the grid, a small-signal model for calculating DC voltage ripple is established, which accurately quantifies the transient and steady-state ripple magnitudes of the capacitor voltage following unbalanced disturbances. Furthermore,

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constraint surfaces for capacitor values under transient/steady-state ripple limits are calculated. Finally, the accuracy of the proposed model is validated through CHIL experiments, and the mechanism of voltage twice-frequency ripple generation in grid-forming inverters is briefly explored. The research conclusions provide valuable insights for DC-link capacitor sizing and can effectively improve the economic performance and power quality of grid-connected inverters.

II. Analysis and Modeling of Voltage Twice-Frequency Ripple under Unbalanced Disturbances

This section first examines the limitations of traditional voltage twice-frequency ripple calculation methods under weak grid conditions, then analyzes the propagation path of unbalanced disturbances in the system, and develops a small-signal model for calculating DC voltage ripple.

A. Limitations of Traditional Methods for Quantifying Voltage Twice-Frequency Ripple:

In the grid-connected inverter system, the twice-frequency ripple in the DC capacitor voltage $v_{2\omega}(t)$ is generated by the twice-frequency component of the system's active power $p_{2\omega}(t)$. When the AC system voltage is in a three-phase unbalanced state, the active power P injected by the inverter into the grid can be expressed as (1).

$$P(t) = P_0 + \underbrace{P_{c2}\cos(2\omega t) + P_{s2}\sin(2\omega t)}_{p_{2\omega}(t)} \tag{1}$$

where P_0 is the DC component of active power, and P_{c2} P_{s2} are the amplitude coefficients of the twice-frequency power components. In steady-state operation of the grid-connected inverter, the DC capacitor C_{dc} typically does not carry the steady-state average power, meaning the DC active component P_0 is usually provided by the upstream machine-side inverter[X]. In this case, C_{dc} is responsible for carrying the twice-frequency component of the active power $p_{2\omega}(t)$, leading to twice-frequency fluctuations in the DC capacitor voltage $v_{2\omega}(t)$. The relationship between $p_{2\omega}(t)$ and $v_{2\omega}(t)$ can be derived using the energy conservation principle for the capacitor over one twice-frequency period. Denoting the amplitude of the voltage twice-frequency component as $V_{2\omega}$and the amplitude of the active power twice-frequency component as $P_{2\omega}$， the energy stored in the capacitor over one twice-frequency period E_c is given by:

$$E_c = \frac{1}{2}C_{dc}(V_{dc}+V_{2\omega})^2 - \frac{1}{2}C_{dc}(V_{dc}-V_{2\omega})^2 \tag{2}$$

Simultaneously, the energy absorbed by the capacitor can also be expressed as the integral of the input active power over time:

$$E_c = \int_{t}^{t+\pi/2\omega} p_{2\omega}(t)\,dt = \int_{t}^{t+\pi/2\omega} P_{2\omega}\cdot\sin(2\omega t)\,dt \tag{3}$$

By combining (2) and (3), the amplitude of the capacitor's twice-frequency voltage $V_{2\omega}$ can be calculated, as shown in (4):

$$V_{2\omega} = \frac{P_{2\omega}}{2\omega V_{dc} C_{dc}} \tag{4}$$

However, the traditional calculation method for voltage twice-frequency ripple based on energy balance within a period has certain limitations. On one hand, $p_{2\omega}(t)$ causes DC voltage ripple $v_{2\omega}(t)$ that directly affects the inverter terminal voltage v_{inv} through the modulation loop. At the same time, $p_{2\omega}(t)$ also influences the inverter reference terminal voltage $v_{inv,ref}$ through the control loop, which then indirectly affects v_{inv}. The above process can be described by (5):

$$v_{inv0} + \Delta v_{inv} = m_a \times (v_{inv,ref0} + \Delta v_{inv,ref}) \times \frac{(V_{dc0} + \Delta V_{dc})}{2} \tag{5}$$

Note that m_a is the SPWM modulation ratio. The change in v_{inv} affects the inverter output current i_{inv}, which ultimately amplifies $p_{2\omega}(t)$, further worsening the DC voltage ripple. The open loop calculation method based on (4) will significantly underestimate the DC voltage ripple level.

On the other hand, with the large-scale integration of renewable energy sources, the grid strength has been gradually decreasing, leading to more frequent weak grid conditions. In weak grids (characterized by SCR<3 according to IEEE Std 1204-1997), the equivalent AC-side impedance is significantly higher than that in strong grids. Consequently, the twice-frequency power ripple $p_{2\omega}(t)$ injected into PCC significantly amplifies the phase fluctuations of the PCC voltage vector $\boldsymbol{V}_{pcc}$, severely affecting the accuracy of the PLL. During unbalanced conditions, the system simultaneously contains the forward rotating positive sequence voltage vector $\boldsymbol{V}_{pcc1}$ and the reverse rotating negative sequence voltage vector $\boldsymbol{V}_{pcc2}$. The superposition of these causes the phase θ_{pcc} of $\boldsymbol{V}_{pcc}$ to fluctuate at twice-frequency, leading to the PLL operating in a weak dynamic state near the stable point θ_{pll0} , as shown in (6). The output phase θ_{pll} of the PLL ultimately influences $v_{inv,ref}$ through *dq* transformation and the control loop, further exacerbating the twice-frequency ripple in the DC voltage.

$$\theta_{pll0} + \Delta\theta_{pll,2\omega} = G_{pll}(s)(\theta_{pcc0} + \Delta\theta_{pcc,2\omega}) \tag{6}$$

In summary, the open-loop calculation method for voltage twice-frequency ripple has certain errors in weak grid conditions. In weak grids, the reduced PLL bandwidth required for stability maintenance prevents accurate phase tracking, causing the system to remain in a continuous weak dynamic state rather than reaching steady state. The persistent twice-frequency ripple in the PLL output phase continuously affects the DC voltage through closed-loop interactions among the modulation loop, control loop, and *dq* transformation, leading to significant underestimation of the actual DC voltage ripple by traditional steady-state calculations. Therefore, it is necessary to fully consider the propagation path of unbalanced disturbances between the inverter and the grid, as well as between the DC and AC systems. A closed-loop small-signal model for the system's imbalance power interaction must be established to accurately quantify the transient and steady-state DC voltage twice-frequency ripple.

B. Analysis of the Propagation Path of Unbalanced Disturbances:

In the following, a single inverter grid connected system is analyzed to illustrate the closed loop propagation path of voltage unbalance disturbances between the inverter and the grid. The system topology is shown in Fig. 1, where the inverter is controlled by voltage oriented control (VOC) and is connected to the grid through the filter inductor L_f. The PCC voltage is denoted by v_{pcc}, and the PCC current by i_{pcc}. The grid is represented by the Thevenin equivalent impedance R_g,

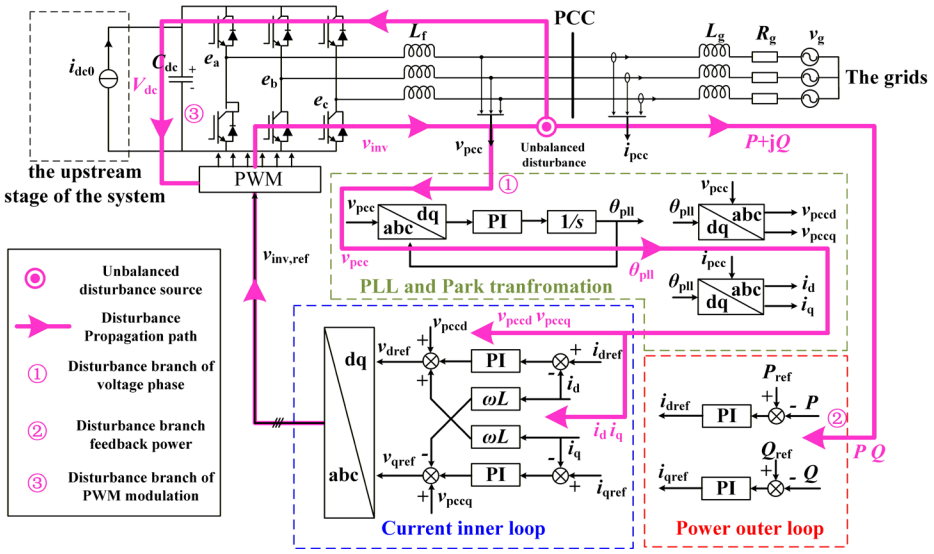

Fig. 1. Topology of a single-inverter grid-connected system.

L_g and the equivalent voltage source v_g. The upper stage system is equivalently modeled as a constant DC current source i_{dc0}, which implies that the DC link capacitor C_{dc} does not carry the DC component of active power.

As shown in Fig. 1, the unbalanced disturbances in the AC system primarily flow into the inverter control loop through three branches, completing the disturbance feedback loop through the inverter terminal output voltage and the grid-connected lines. First, the positive and negative sequence voltages caused by grid voltage unbalance result in twice-frequency fluctuations in both the amplitude and phase of the PCC voltage vector. The PCC voltage phase is estimated andoutput by the PLL, serving as the reference phase θ_{pll} for the inverter control loop's dq transformation, affecting the magnitude of the feedforward voltages v_d, v_q and feedback currents i_d, i_q. This propagation path is shown as branch ① in Fig. 1. Next, the unbalanced disturbance induces twice-frequency fluctuations in the system's active and reactive power, affecting the feedback power P, Q in the power outer loop, which in turn influences the current inner loop reference values i_{dref}, i_{qref}. This is shown in branch ② of Fig. 1. These disturbance paths ① and ② jointly modify the inverter terminal voltage reference values v_{dref}, v_{qref} in the current inner loop. Finally, the twice-frequency ripple caused by active power fluctuations alters the DC capacitor voltage ripple, changing the magnitude of the DC modulation voltage V_{dc}, as shown in branch ③ of Fig. 1. The three disturbance paths ultimately affect the inverter terminal voltage v_{inv} through the PWM modulation loop, which, through the transmission line, influences the PCC voltage and current, completing the closed-loop of the unbalanced disturbance. During asymmetrical faults, these three dynamic loops continuously interact, causing the system to remain in a weak dynamic state, leading to errors in the traditional open-loop voltage ripple calculation method.

C. Modeling of Voltage Phase Disturbance Branch:

The voltage phase of the unbalanced PCC voltage vector θ_{pcc}, after being estimated by the PLL, serves as the reference phase θ_{pll} for the coordinate transformation of both the feedforward voltage v_{pcc} and the feedback current i_{pcc}. At the same time, the unbalanced disturbance directly influences the magnitude of v_{pcc} and i_{pcc}. These two paths ultimately lead to changes in the dq-axis feedforward voltages v_{pccd}, v_{pccq} and the feedback currents i_d, i_q. The expression for the dq-axis feedforward voltage is as follows:

$$\begin{cases} v_{pccd} = V_{pcc}\cos\left(\theta_{pcc}-\theta_{pll}\right) \\ v_{pccq} = V_{pcc}\sin\left(\theta_{pcc}-\theta_{pll}\right) \end{cases} \tag{7}$$

It should be noted that, during the transient process following the unbalanced disturbance, the PLL cannot instantaneously respond to phase jumps, meaning θ_{pcc} is not equal to θ_{pll} during the transient phase. This process can be described by the PLL phase transfer function:

$$G_{pll}(s) = \frac{\Delta\theta_{pll}(s)}{\Delta\theta_{pcc}(s)} = \frac{K_{pllp}s + K_{plli}}{s^2 + V_{pcc}(K_{pllp}s + K_{plli})} \tag{8}$$

Where K_{pllp} and K_{plli} are the proportional and integral coefficients of the PI controller in the PLL control structure, respectively. By linearizing the feedforward voltage expression in (7) and substituting the PLL phase transfer function from (8), we obtain:

$$\begin{bmatrix} \Delta v_{pccd} \\ \Delta v_{pccq} \end{bmatrix} = \mathbf{H}_{fe} \begin{bmatrix} \Delta\theta_{pcc} \\ \Delta V_{pcc} \end{bmatrix} \tag{9}$$

Equation (9) represents the small-signal model of the feedforward voltage disturbance branch. The effect of the unbalanced disturbance on the feedback current is consistent with that on the feedforward voltage, and thus will not be further discussed here.

D. Modeling of Feedback Power Disturbance Branch:

The positive sequence and negative-sequence voltage and current components caused by the unbalanced disturbance generate twice-frequency ripples in the system's active and reactive power, which affect the feedback powers P and Qin the power outer loop, further influencing the current inner loop reference values i_{dref} and i_{qref}, as shown in(10)

$$\begin{bmatrix} \Delta i_{dref} \\ \Delta i_{qref} \end{bmatrix} = \mathbf{H}_{po} \begin{bmatrix} \Delta P_{ref} - \Delta P \\ \Delta Q_{ref} - \Delta Q \end{bmatrix} \tag{10}$$

Note that $\mathbf{H_{po}}$ is the transfer function matrix of the power outer loop. Considering that when the inverter power reference values are constant, $\Delta P_{ref}=\Delta Q_{ref}=0$, by combining (10) with the calculation expressions of P and Q in the dq-axis, the small-signal model of the feedback power disturbance branch is obtained, as shown in (11).

$$\begin{bmatrix}\Delta i_{dref}\\ \Delta i_{qref}\end{bmatrix}=\mathbf{H_{vp}}\begin{bmatrix}\Delta v_{pccd}\\ \Delta v_{pccq}\end{bmatrix}+\mathbf{H_{ip}}\begin{bmatrix}\Delta i_{d}\\ \Delta i_{q}\end{bmatrix} \tag{11}$$

The unbalanced disturbance branches ① and ② ultimately construct the inverter terminal voltage reference values v_{dref} and v_{qref} in the current inner loop. The linearized expression of the current inner loop is shown in (12):

$$\begin{bmatrix}\Delta v_{invd,ref}\\ \Delta v_{invq,ref}\end{bmatrix}=\begin{bmatrix}\Delta v_{pccd}\\ \Delta v_{pccq}\end{bmatrix}+\mathbf{H_{ci}}\begin{bmatrix}\Delta i_{dref}\\ \Delta i_{qref}\end{bmatrix}-\mathbf{H_{cid}}\begin{bmatrix}\Delta i_{d}\\ \Delta i_{q}\end{bmatrix} \tag{12}$$

Note that $\mathbf{H_{ci}}$ is the transfer function matrix of the current inner loop, and $\mathbf{H_{cid}}$ is the decoupling transfer function matrix of the current inner loop.

E. Modeling of PWM Modulation Disturbance Branch:

The twice-frequency ripple in active power causes fluctuations in the DC capacitor voltage V_{dc}. By linearizing the capacitor energy balance equation, we obtain:

$$\Delta P=C_{dc}V_{dc0}\omega_0\Delta V_{dc} \tag{13}$$

Next, the inverter modulation loop converts the DC capacitor voltage V_{dc} and the reference voltage $v_{inv,ref}$ into the terminal voltage v_{inv}, as shown in (14):

$$\Delta v_{inv}=\frac{m_a}{2}\times(v_{inv,ref0}\Delta V_{dc}+V_{dc0}\Delta v_{inv,ref}) \tag{14}$$

The inverter terminal voltage v_{inv}, through the grid-connected line, further causes changes in the line current, voltage, and transmitted power. This process can be described by the AC system's circuit equation (15):

$$\begin{bmatrix}\Delta v_{invd}\\ \Delta v_{invq}\end{bmatrix}=\mathbf{Z_f}\begin{bmatrix}\Delta i_{d}\\ \Delta i_{q}\end{bmatrix}+\begin{bmatrix}\Delta v_{pccd}\\ \Delta v_{pccq}\end{bmatrix}=\mathbf{Z_{grid}}\begin{bmatrix}\Delta i_{d}\\ \Delta i_{q}\end{bmatrix} \tag{15}$$

In (19), $\mathbf{Z_f}$ and $\mathbf{Z_{grid}}$ are the grid-connected line impedance matrix and the AC side equivalent impedance matrix, respectively. By combining the linearized expressions from the current inner loop (12), modulation equation (14), power disturbance branch (11), capacitor energy balance (13), and grid-connected line (15), the closed-loop small-signal equation for the DC capacitor voltage is derived as (16).

$$\Delta V_{dc}=\frac{\mathbf{H_{li}H_{cu}H_{fe}}}{\omega_0 C_{dc}V_{dc0}(\mathbf{H_{li}H_{cu}H_{fp}}+\mathbf{H_{li}H_{mo}}+\mathbf{I}_{2*2})}\begin{bmatrix}\Delta\theta_{pcc}\\ \Delta V_{pcc}\end{bmatrix} \tag{16}$$

Matrices $\mathbf{H_{cu}}$, $\mathbf{H_{li}}$, $\mathbf{H_{fp}}$, and $\mathbf{H_{mo}}$ can be derived from the previously mentioned matrices, with the derivation process omitted. The closed-loop transfer function block diagram of the unbalanced disturbance is shown in Fig. 2.

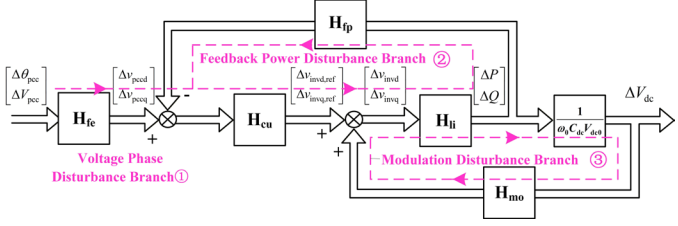

Fig. 2. Block diagram of closed-loop transfer function for unbalanced disturbance.

III. Model Application - Capacitor Value Constraint Calculation

Currently, there are no explicit regulations specifying the magnitude of the DC capacitor voltage ripple level δ. In general industrial applications, the steady state ripple ratio limit is typically between 2% and 5%, while the transient ripple ratio limit is between 8% and 10% [8]. In this section, a conservative choice is made with the steady-state ripple constraint δ_{ss}<2% and the transient ripple constraint δ_{tr}<8%. By rearranging both sides of equation (16), the capacitor size constraint equation for different levels of imbalance can be obtained, as shown in (17).

$$C_{dc}=\frac{\mathbf{H_{fe}H_{li}H_{cu}}}{\omega_0 V_{dc0}{}^2\delta(\mathbf{H_{li}H_{cu}H_{fp}}+\mathbf{H_{li}H_{mo}}+\mathbf{I}_{2*2})}\begin{bmatrix}\Delta\theta_{pcc}\\ \Delta V_{pcc}\end{bmatrix} \tag{17}$$

By substituting the steady-state ripple constraint and the transient ripple constraint into (17), the minimum value of the DC capacitor Cdc,min is taken as the larger of the transient capacitor minimum value Ctr,min and the steady-state capacitor minimum value Css,min. By varying K_{Op} and K_{Ip}, the power outer loop control parameters, along with the inverter reference powers P_{ref} and Q_{ref}, the grid imbalance ε_{PVUR}, and the grid-side inductance L_g , the capacitor value transient/steady-state ripple constraint surface and feasible region can be obtained, as shown in Fig. 3. In Fig. 3, the upper space above the union of the transient constraint minimum capacitor surface Ctr,min and the steady-state constraint minimum capacitor surface Css,min represents the feasible region for the capacitor value $C_{feasible}$.

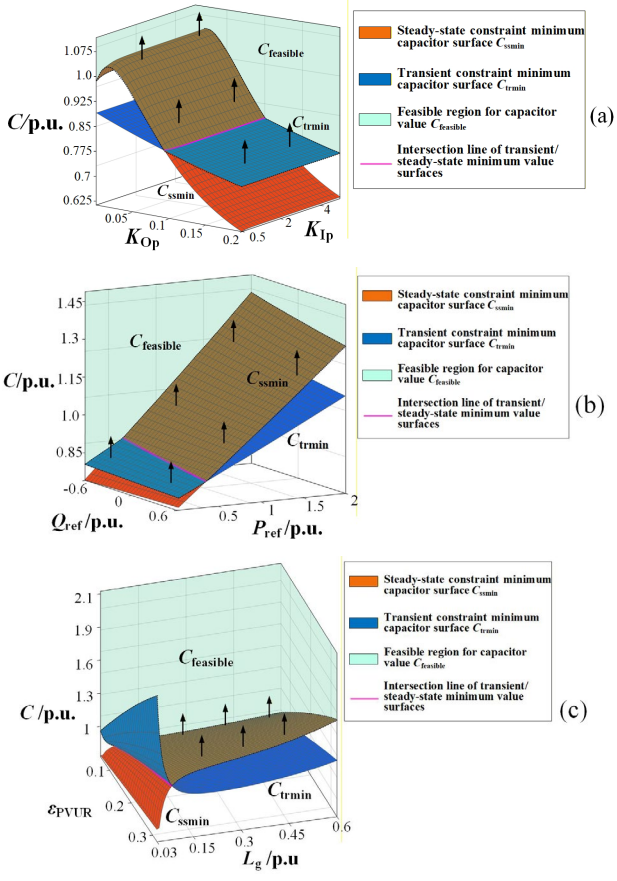

Fig. 3. (a) Feasible region for capacitor value under different power outer loop control parameters. (b) Feasible region for capacitor value under different power reference values. (c) Feasible region for capacitor value under different levels of unbalance and grid strength

Fig. 3(a) shows the feasible region for capacitor value under varying power outer loop control parameters K_{Op} and K_{Ip}. Analysis reveals that as the power outer loop proportional coefficient K_{Op} decreases, both the transient and steady-state minimum capacitor values significantly increase. However, as the current inner loop proportional coefficient K_{Ip} decreases, the transient and steady-state minimum capacitor values only slightly increase. This is because a decrease in the power outer loop proportional coefficient K_{Op} significantly increases the voltage twice-frequency ripple, requiring a larger DC capacitor to meet the ripple constraint conditions. The bandwidth of the current inner loop has a less significant impact on the capacitor's twice-frequency ripple, and changes in K_{Ip} have little effect on the feasible region for the capacitor value. Furthermore, there exists an intersection line between the transient constraint minimum capacitor surface $C_{tr,min}$ and the steady-state constraint minimum capacitor surface $C_{ss,min}$ indicating that, under conditions with a large K_{Op}, the transient ripple constraint δ_{tr}<8% is the more stringent constraint. As K_{Op} decreases further, the steady-state ripple constraint δ_{ss}<2% becomes the effective constraint boundary. The analysis for Fig. 3(b) and 3(c) is similar to that of Fig. 3(a) and will not be discussed further.

IV. Experimental Validation and Results

The system with the topology shown in Fig. 1 was run on the CHIL experimental platform. The DC voltage waveform of the inverter was measured after unbalanced disturbances and compared with the results from the proposed model and traditional open-loop calculations to verify the accuracy of the model. In the experimental setup, the grid-side inductance is L_g = 20 mH and the rated power is P_{ref} = 8 kW, resulting in a SCR of approximately 2.97, which characterizes a weak grid condition. At t=20s, the AC grid-side voltage v_a drops to 20% of its rated value, the inverter DC voltage waveform from the experiment and the calculated waveform are shown in Fig. 4.

Comparing Fig. 4(a), (b), and (c), it can be seen that the inverter DC capacitor voltage transient ripple is ΔV_{tr1}≈34V and the steady-state voltage ripple is ΔV_{ss1}≈28V. The proposed model calculates the transient voltage ripple as ΔV_{tr2}=34.5V and the steady-state voltage ripple as ΔV_{ss2}=27.9V. The traditional open-loop calculation method yields a transient voltage ripple of ΔV_{tr3}=27.1V and a steady-state voltage ripple of ΔV_{ss3}=21.4V. The proposed model reduces the transient voltage ripple calculation error by 18.8% and the steady-state active ripple calculation error by 20.3%.

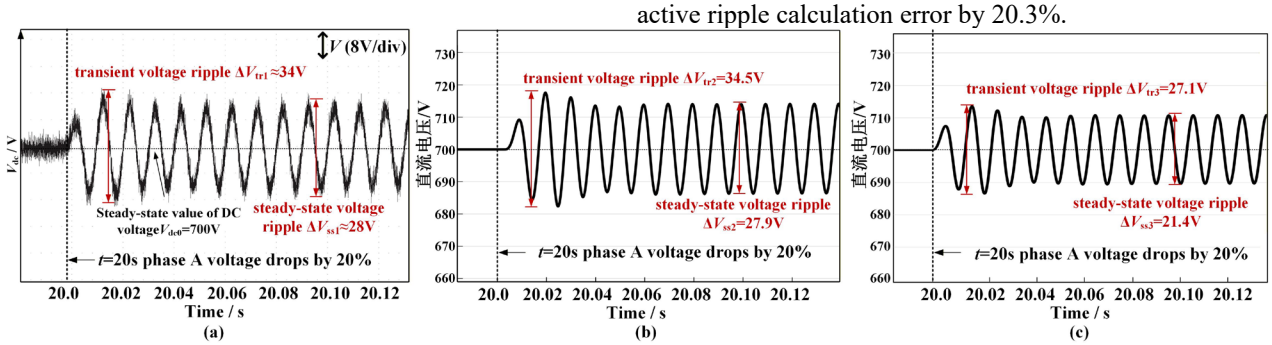

Fig. 4. Inverter DC voltage waveforms: (a) CHIL experimental results, (b) results from the proposed model, (c) traditional open-loop calculation results

V. Conclusion and Future Work

This study mainly discusses the mechanism and quantitative analysis of DC capacitor voltage ripple generation in grid-following inverters under unbalanced disturbances. As the penetration of low-inertia power electronic equipment in power systems increases, grid-forming inverters are receiving increasing attention for their reliable voltage and frequency support capabilities. Unlike grid-following inverters, grid-forming inverters have a disturbance channel from active power to frequency, where unbalanced disturbances can directly affect the system's voltage and frequency. This results in a more complex mechanism for DC capacitor voltage ripple generation in grid-forming inverters, which will be further investigated in future research.

VI. References

[1] X. Chen, S. Bu, and I. Kocar, "Grid-Forming IBRs under Unbalanced Grid Conditions: Challenges, Solutions, and Prospects," *IEEE Trans. Sustain. Energy*, pp. 1–16, 2025.

[2] A. Safayet, M. Islam, and T. Sebastian, "Comprehensive Analysis for DC-Link Capacitor Sizing for a Three-Phase Current-Controlled Voltage-Source Inverter," *IEEE Trans. on Ind. Applicat.*, vol. 58, no. 4, pp. 4248–4260, July 2022.

[3] X. Pei, W. Zhou, and Y. Kang, "Analysis and Calculation of DC-Link Current and Voltage Ripples for Three-Phase Inverter With Unbalanced Load". *IEEE Trans. Power Electron.*, VOL. 30, NO. 10. 5401–5412, October 2015.

[4] S. Bhowmick, D. Mukherjee, T. S. Basu, and C. Chakraborty, "A Three-Phase Four-Leg Neutral-Point-Clamped Photovoltaic Inverter With Decoupled Active and Reactive Power Control and DC-Link Voltage Ripple Minimization Under Unbalanced Grid Operation," *IEEE Trans. Power Electron.*, vol. 40, no. 6, pp. 7829–7843, June 2025.

[5] A. M. Cross, P. D. Evans, and A. J. Forsyth, "DC link current in PWM inverters with unbalanced and non-linear loads," *Proc. IEE*, vol. 146, no. 6, pp. 620–626, Nov. 1999.

[6] I. Ziyat, J. Wang, and P. R. Palmer, "Voltage Ripple Model and Capacitor Sizing for the Three-Phase Four-Wire Converter Used for Power Redistribution," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 12, no. 2, pp. 1437–1445, Apr. 2024.

[7] S. Guenter, J. Yang, G. Buticchi, F. W. Fuchs, and M. Liserre, "DC-Link Voltage Dynamics of Three-Level Four-Wire Grid-Connected Converters During Harmonics Injection Operations," *IEEE Trans. Ind. Electron.*, vol. 70, no. 8, pp. 8000–8008, Aug. 2023.

[8] M. Vujacic, O. Dordevic, R. Mandrioli, and G. Grandi, "DC-link low-frequency current and voltage ripple analysis in multiphase voltage source inverters with unbalanced load," *IET Electric Power Appl*, vol. 16, no. 3, pp. 300–314, Mar. 2022.

[9] Z. Shuai, Y. Peng, J. M. Guerrero, Y. Li, and Z. J. Shen, "Transient Response Analysis of Inverter-Based Microgrids Under Unbalanced Conditions Using a Dynamic Phasor Model," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2868–2879, Apr. 2019.