Detailed Equivalent Model for Parallel CPU-GPU EMT-type Simulation of Solid-State Transformer

Walid Hatahet
School of Engineering
The University of British Columbia
Kelowna, Canada
walid.hatahet@ubc.ca

Hengyu Li
School of Engineering
The University of British Columbia
Kelowna, Canada
hengyu.li@ubc.ca

Liwei Wang
School of Engineering
The University of British Columbia
Kelowna, Canada
liwei.wang@ubc.ca

Juan Páez Alvarez
OPAL-RT Technologies
Montreal, Canada
juan.paez-alvarez@opal-rt.com

***Abstract*—Solid-state transformer (SST) enables the efficient interface between AC grids and the DC distribution networks. Detailed modeling of numerous components in the power converter system requires massive computational resources. This paper proposes a numerically efficient decoupled detailed equivalent model (DEM) of the SST for efficient electromagnetic transient (EMT) simulation. The proposed model can accurately represent the fast dynamics of the converter system under normal, transient, and IGBT-blocked states. In addition, a switching interpolation technique is employed to ensure compensation of intra-time-step switching events and convergence of the simulation results with relatively large time step-sizes. To further accelerate the EMT simulation, a parallel simulation algorithm is developed to utilize the computational resources of both central and graphics processing units (CPU-GPU). The accuracy of the proposed DEM is validated against the detailed model (DM) of SST system, while the efficiency of the parallel algorithm is assessed by comparison with a CPU-only implementation.**

Keywords—Electromagnetic transient, equivalent circuit model, graphics processing unit, solid-state transformer, switching interpolation.

I. INTRODUCTION

Solid-state transformer (SST) is emerging as key component to interface systems with various voltage levels and enable bidirectional power flow capabilities between medium-voltage AC (MVAC) grids and low-voltage DC (LVDC) networks [1]. The use of SST has become substantial in many applications, including ultra-fast charging stations for electric-vehicles, renewable energy resources, and the integration of DC microgrids and distribution networks to the AC grids. In SST, the dual-active-bridge (DAB) converter offers galvanic isolation and fine-grained controllability that conventional line-frequency transformers cannot provide. However, the input-series-output-parallel (ISOP) configuration leads to complexities in the SST design when compared to other voltage-source converter topologies.

Significant hurdles arise when simulating the SST converter system in normal and faulted modes. The large number of nodes count results in a large-scale and time-varying conductance G-matrix of the nodal equation in electromagnetic transient (EMT) simulation [2]. In addition, the complex circuit topology and various switching frequencies in the SST require fine time step-sizes and frequent matrix refactorizations in the EMT simulation. Consequently, conventional EMT models of SST become computationally expensive, highlighting the need for efficient equivalent-circuit modeling. Recent advances in SST converter system motivate the acceleration of its EMT simulation. In [3], each DAB's isolation transformer is discretized into a two-port Norton equivalent circuits, resulting in an accelerated detailed equivalent model (DEM) of the ISOP-SST. The work in [4] focuses on decoupling the DAB circuit through the medium-frequency transformer (MFT) in the SST. These DEMs can achieve node reduction and accelerated EMT simulation of the SST. However, complex formulation of the module conductance G-matrices and the time-variant elements impose high computational burdens.

The work in [5] presents a DEM with reduced order of the nodal admittance matrix for modular power electronics transformer (PET)-based systems. The EMT simulation is accelerated by using multicore central processing unit (CPU) parallelization. In [6], a cut-set-matrix-based decoupling method is presented, alongside a multicore CPU parallelization algorithm, to improve the simulation efficiency of the SST. While [5] and [6] seek faster simulation, frequent nodal conductance matrix refactorization is required due to the two-value resistor representation of IGBT switches. Moreover, multicore CPU parallelization can only achieve partial simulation speed-ups due to its serial-processing nature, limited concurrency, and substantial inter-core synchronization overheads. Field-programable gate array (FPGA) is presented in [7] to develop an accelerated platform for parallel real-time simulation of cascaded SST. While the FPGA offers a high-speed simulation platform, scaling to large converter systems is cost prohibitive.

Other works proposed the graphics processing unit (GPU) as an efficient alternative platform to multicore CPUs or FPGAs. The work in [8] presents the co-simulation of component-level thermo-electromagnetic transient modeling of SST on the GPU. In [9], the massive parallel processing capabilities of GPUs are leveraged to speed up the computation-intensive simulation of

979-8-3315-8138-1

modular multilevel converter (MMC) systems.

This paper focuses on enhancing the numerical accuracy and efficiency of EMT-type simulation for the SST. A fully decoupled DEM is proposed for the SST, which achieves a reduced node count in the network solution and constant G matrix. The proposed DEM can accurately represent the dynamics of the SST under normal, transient, and blocked modes. In addition, a switching interpolation technique is proposed to accurately compensate for the intra-step switching events and enable larger time step-sizes for accelerated simulation. Furthermore, a parallel CPU-GPU platform is developed to enable high-speed EMT simulation of the SST.

II. SST Detailed Equivalent Model

This section presents the three-phase multimodule SST and the proposed decoupled switching function-based DEM. The proposed DEM offers a decoupled circuit representation with reduced nodes count and a constant conductance matrix of the SST. Furthermore, switching interpolation technique is introduced to enhance the accuracy of the proposed DEM.

A. Three-phase Multimodule SST

The circuit diagram of the three-phase multimodule SST is illustrated in Fig. 1. Each phase of the SST consists of two stages (i.e., Stage-I and Stage-II), following the ISOP configuration.

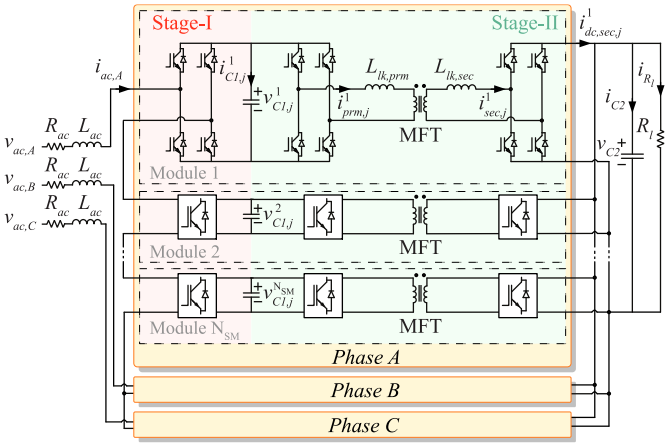

Fig. 1. Three-phase multimodule SST circuit diagram.

Stage-I of the SST comprises multiple series-connected full-bridge (FB) modules, which interface the medium-voltage AC (MVAC) grid with the medium-voltage DC (MVDC) network. On the MVAC side, $v_{ac,j}$ represents the three-phase grid voltages, where j represents the phase number (i.e., $j \in \{A, B, C\}$). On the MVDC side, the DC-link capacitor voltage and the current of the i^{th} submodule are denoted as $v^i_{C1,j}$ and $i^i_{C1,j}$, respectively. A real-reactive (PQ)-control scheme is adopted to synthesize the modulation signals that are used to generate the gating pulses for the FBs in Stage-I. To ensure proper operation of the SST, a voltage balancing control (VBC) strategy is employed to sort the submodule voltages in each phase and maintain the MVDC-link energy balance.

Stage-II consists of N_{SM} DAB modules, which interface the MVDC-link with the low-voltage DC (LVDC)-link. Each DAB incorporates a medium-frequency transformer (MFT) that provides galvanic isolation and voltage matching between the MVDC and LVDC ports. $i^i_{prm,j}$ and $L_{lk,prm}$ represent the primary-side AC current and leakage inductance, respectively, whereas $i^i_{sec,j}$ and $L_{lk,sec}$ represent their secondary-side counterparts. On the LVDC side, all DABs are connected in parallel with the common LVDC-link capacitor C_2 with voltage and current denoted as v_{C2} and i_{C2}, respectively. A resistive load R_l is connected in parallel across the LVDC terminal. The phase-shifted PWM is used to control the power flow between the primary- and secondary-side of the DAB and generate the gating pulses for the FBs in Stage-II.

B. Decoupled Detailed Equivalent Model

In order to achieve constant conductance G matrices of the SST, the DEM of the SST is presented in this subsection, as depicted in Fig. 2. The proposed DEM uses switching function to represent the semiconductor switching status of FB converters in Stage-I or Stage-II of the SST.

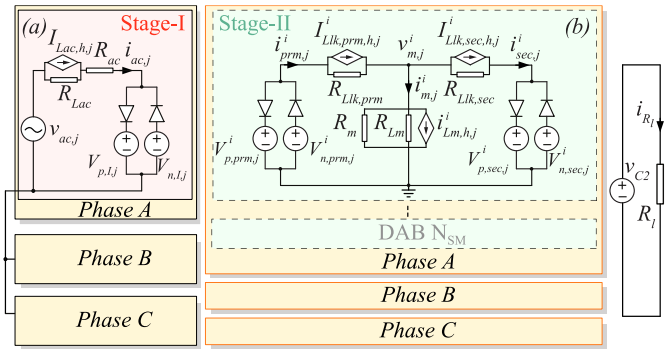

Fig. 2. SST decoupled DEM. (a) Equivalent circuit of AC/DC converter in Stage-I. (b) Equivalent circuit of DABs in Stage-II.

In each phase, the SST modules can be decoupled through the MVDC-link capacitors. An explicit integration rule, i.e., Adams-Bashforth 2nd order method, is used to discretize the voltages of the MVDC-link capacitors based on the historical values from two previous time steps, and are derived as

$$v^i_{C1,j}(t+\Delta t) = v^i_{C1,j}(t) + \frac{\Delta t}{C_1}\left(\frac{3}{2} i^i_{C1,j}(t) - \frac{1}{2} i^i_{C1,j}(t-\Delta t)\right) \quad (1)$$

where Δt is the discretization time step-size. The MVDC-link capacitor currents can be obtained as

$$i^i_{C1,j} = S^i_{I,j} i_{ac,j} - S^i_{prm,j} i^i_{prm,j} \quad (2)$$

where $S^i_{I,j}$ and $S^i_{prm,j}$ take values in $\{1, -1, 0\}$, denoting the switching functions of the i^{th} Stage-I FB and Stage-II DAB primary-side, respectively. These values correspond to the positive insertion, negative insertion, and bypass modes.

Similarly, on the MVDC side, the SST modules are decoupled from the load R_l at the LVDC-link capacitor C_2, using the Adams-Bashforth 2nd order method as

$$v_{C2}(t+\Delta t) = v_{C2}(t) + \frac{\Delta t}{C_2}\left(\frac{3}{2} i_{C2}(t) - \frac{1}{2} i_{C2}(t-\Delta t)\right) \quad (3)$$

where the LVDC-link capacitor current is calculated as

$$i_{C2} = \sum_{j=A,B,C} \sum_{i=1}^{N_{SM}} S^i_{sec,j} i^i_{sec,j} - \frac{v_{C2}}{R_l} \quad (4)$$

where $S^i_{sec,j} \in \{1, -1, 0\}$ is the switching function of the DABs

secondary-side in Stage-II.

As shown in Fig. 2(a), the AC terminal voltages of Stage-I FBs are modeled by positive and negative equivalent AC voltage sources, $V_{p,I,j}$ and $V_{n,I,j}$, in series with an anti-parallel diode pair [10], and in deblocking mode are expressed as

$$V_{p,I,j} = V_{n,I,j} = \sum_{i=1}^{N_{SM}} S_{I,j}^{i} v_{C1,j}^{i} \quad (5)$$

while in blocking mode, these equivalent voltage sources are derived as

$$\begin{cases} V_{p,I,j} = \sum_{i=1}^{N_{SM}} v_{C1,j}^{i} \\ V_{n,I,j} = -\sum_{i=1}^{N_{SM}} v_{C1,j}^{i} \end{cases} \quad (6)$$

Similarly, as shown in Fig. 2(b), the AC terminals of stage-II DABs can be modeled by positive and negative equivalent AC voltage sources. Their expressions for different operating modes are summarized in Table I.

TABLE I
EQUIVALENT VOLTAGE SOURCES OF DAB IN STAGE II

Mode	Primary-side		Secondary-side	
	$V_{p,prm,j}^{i}$	$V_{n,prm,j}^{i}$	$V_{p,sec,j}^{i}$	$V_{n,sec,j}^{i}$
Deblock	$S_{prm,j}^{i} v_{C1,j}^{i}$	$S_{prm,j}^{i} v_{C1,j}^{i}$	$S_{sec,j}^{i} v_{C2}$	$S_{sec,j}^{i} v_{C2}$
Block	$v_{C1,j}^{i}$	$-v_{C1,j}^{i}$	v_{C2}	$-v_{C2}$

C. Switching Interpolation Techinque

The EMT-type simulation of power electronic converters typically relies on fixed time-step solvers. However, switching events often occur between two consecutive time steps and not exactly at the discretized integer time steps. To address this issue, this subsection introduces a switching interpolation technique. The proposed method compensates for intra-step switching events to enhance numerical accuracy.

As an illustrative example, a single-phase FB converter with a capacitor on the DC-side with voltage v_C and an inductor L as a load on the AC-side with inductor current i_{AC}. The AC output voltage on the inductor side can be expressed as

$$v_{AC} = S \cdot v_c \quad (7)$$

where S takes the value of 1 or -1, corresponding to positive or negative insertion modes, depending on the comparison between the modulation signal $m(t)$ and the carrier signal $C(t)$, illustrated in Fig. 3(a).

As shown in Fig. 3(b), the switching function S without switching interpolation can only change at discrete time steps (e.g., the next time step t_{k+1}), represented by the red dotted curve. This leads to a misrepresentation of the actual switching instant at t_z, denoted by the blue solid curve. The yellow shaded regions in the subplots of S and i_{AC}, shown in Fig. 3(b) and (d), illustrate the simulation errors caused by inaccurate representation of switching event and incorrect integration of the inductor voltage v_{AC} during the transition from the present time step t_k to the next time step t_{k+1}.

The effect of intra-step switching of the single-phase FB converter on the AC-side inductor L is compensated using the fast average of AC voltage at the time interval $[t_k, t_{k+1}]$ as

$$v_{AC,avg} = m_d \cdot v_c \quad (8)$$

where m_d is the average modulation ratio and is expressed as

$$m_d = 2\frac{t_{on}}{\Delta t} - 1 \quad (9)$$

where t_{on} is the actual on-time of the switch, and Δt is the simulation time step-size. Now, the AC inductor current can be accurately calculated after the compensation of the intra-step switching events, as shown by the cyan dotted curve in Fig. 3(d). This technique can be used for the FBs in stage-I and stage-II of the SST submodules presented in previous subsection and replace switching functions in (2), (4), (5), and Table I.

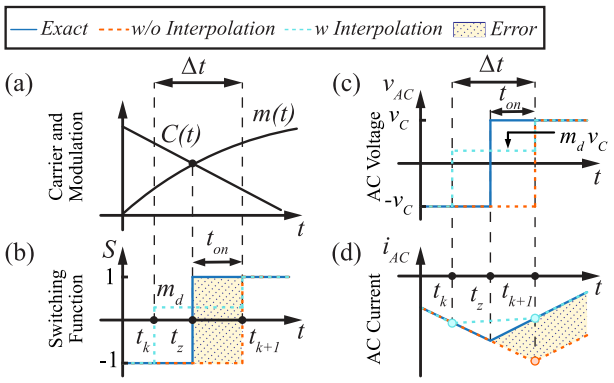

Fig. 3. Switching interpolation technique for a single-phase FB converter. (a) Carrier and modulation signals. (b) Switching function. (c) FB AC voltage. (d) FB AC current.

III. PARALLEL CPU-GPU SIMULATION PLATFORM

The implementation of GPU-accelerated EMT-type simulation platform for the SST relies on careful mapping and scheduling of computational tasks. The independent parallel workloads of the EMT algorithm are executed on the GPU, while the sequential computations are handled by the CPU. The CPU-GPU platform is built on Intel i7- CPU (16 GB RAM), paired with an NVIDIA RTX-2060 GPU.

Fig. 4 illustrates the flowchart of the SST model in CUDA EMT-type simulation. Computations with serial nature are carried out on the CPU where it has minimal latency of serial computations. On the other hand, independent tasks are moved to the GPU kernel to be processed in parallel. When the SST simulation program starts, memory subroutines are carried out. Then, the PQ-control along with the MVDC energy balancing control are executed on the CPU. The MVDC energy balancing control ensures the MVDC bus voltage balance by tuning the PQ commands. These controllers are inherently serial in nature. Therefore, CPU can perform the associated calculations efficiently within a few microseconds. However, when computing the states of multiple modules across different SST phases, the presence of nested loops makes the CPU execution less efficient. There, a GPU kernel is launched to process the modules of each SST phase in parallel, with individual modules mapped to separate CUDA threads.

Within each simulation cycle, necessary data are loaded from the GPU global memory to the thread-block shared memory. Then, MVDC capacitors are sorted in parallel. Within each thread, switching interpolation for Stages-I and -II are computed, enabling the solution of each module and the update of DAB voltages and currents and the MVDC capacitor voltage v_{C1}. Parallel thread reduction within each thread-block is

carried out to efficiently calculate the arm voltage v_{arm} and summation of secondary-side DC currents $i_{dc,sec,\Sigma}$ that are necessary to update the network solution in the next time step. The summation of MVDC capacitor voltages $v_{C1,\Sigma}$, necessary for the MVDC balancing controller, is carried out on the GPU using the parallel reduction technique. Finally, arm currents $i_{ac,j}$ and LVDC voltage v_{C2} are updated on the CPU main thread by solving the SST network.

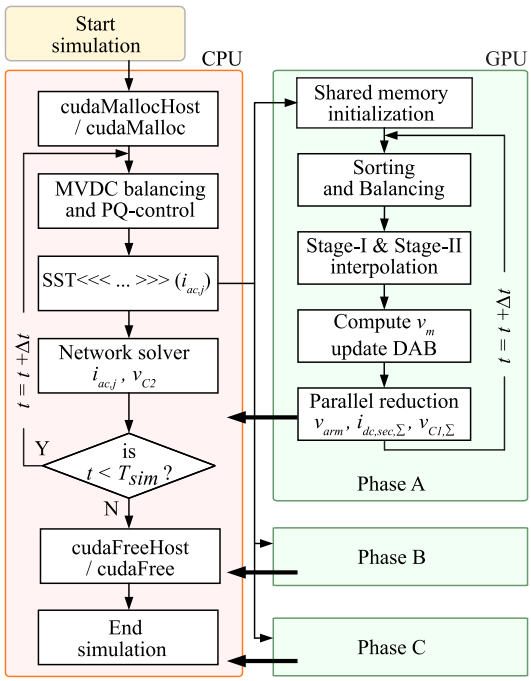

Fig. 4. Flowchart of the SST model in CUDA EMT-type simulation program.

IV. Simulation Studies

In this section, the numerical accuracy of the proposed CPU-GPU DEM of SST with switching interpolation is evaluated by comparison with the DM implemented in Simulink/Simscape Electrical toolbox. The DM employs a fixed-step discrete solver with a fine time step-size of 1µs. The proposed DEM is simulated with a large time step of 10µs. In this SST test system, Stage-I carrier frequency is 5kHz, while Stage-II DAB switching frequency is 2kHz.

A. Steady State and Active Power Change Operation

In this subsection, an active power variation scenario is studied to verify the numerical accuracy of the proposed SST DEM in comparison with the DM. In the case study, each converter stage of the DM and DEM consists of 5 modules per phase. The real power reference is initially set to 1 p.u. At $t = 4s$, the reference is reduced to 0.6 p.u.

As shown in Fig. 5(a) the summation of MVDC-link capacitor voltages drops instantly due to the power reduction. Fig. 5(b) demonstrates that the LVDC-link voltage magnitude decreases instantaneously at $t = 4s$ but gradually recovers to its rated value. Fig. 6(b) shows the arm currents of the three phases are reduced at $t = 4s$ due to the change in real power reference. The simulation results in Figs. 5 and 6 demonstrate high accuracy of the proposed DEM compared to the DM.

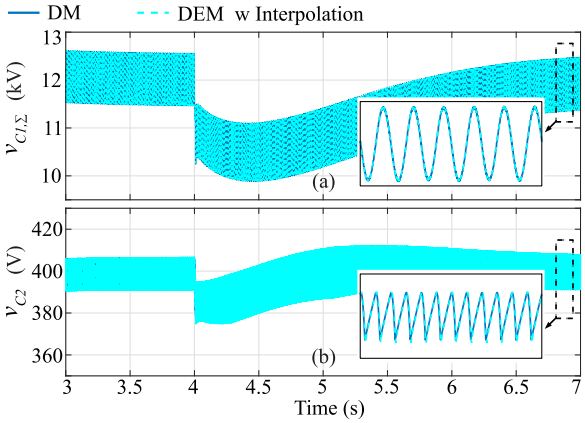

Fig. 5. DC-link voltages of SST. (a) Summation of MVDC-link capacitor voltages in stage-I of phase A. (b) LVDC-link voltage in stage-II.

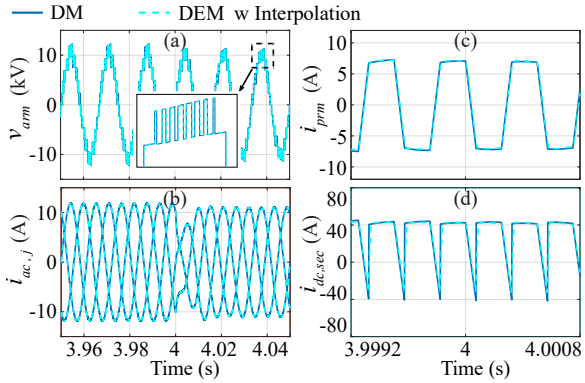

Fig. 6. SST voltages and currents. (a) Arm voltage of phase A. (b) Arm currents. (c) DAB primary AC and (d) secondary DC currents of 1st module in phase A.

B. LVDC Pole-to-pole Fault Simulation

In this case study, a DC fault occurs at the LVDC-link. The IGBTs of the SST are blocked during the fault, and the direction of converter currents is determined by the diodes in the FBSMs. The summation of MVDC-link capacitor voltages in Stage I remains constant during the fault as shown in Fig. 7(a). In Stage II, when the DC-fault occurs, LVDC-link voltage reduces to zero as shown in Fig. 7(b). The primary- and secondary-side currents become zero when the DC fault is detected and all the FBSMs are blocked, as shown in Fig. 7(c) and (d).

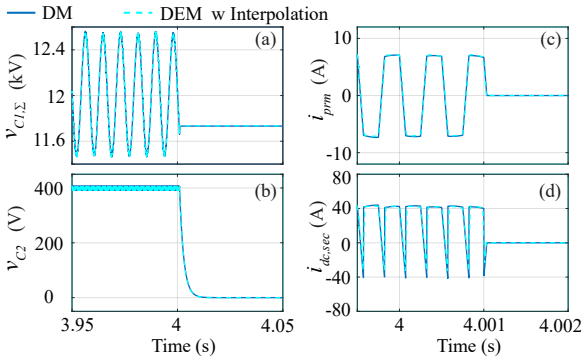

Fig. 7. Simulation results of LVDC-link pole-to-pole fault operation. (a) Summation of MVDC-link capacitor voltages in Stage I of phase A. (b) LVDC-link voltage in Stage II. (c) DAB primary AC and (d) secondary DC currents of the 1st module in phase A.

C. Verification of Switching Interpolation

This case study validates the effectiveness of the switching

interpolation technique. The same DM in previous case study is used to assess the accuracy of both DEMs with and without switching interpolation as shown in Figs. 8 and 9.

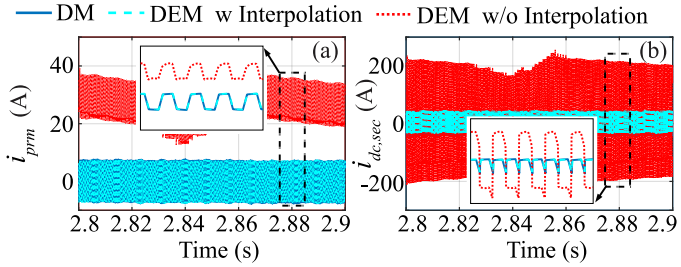

Fig. 8. Validation of switching interpolation technique. (a) DAB primary AC and (b) secondary DC currents of 1st module in phase A.

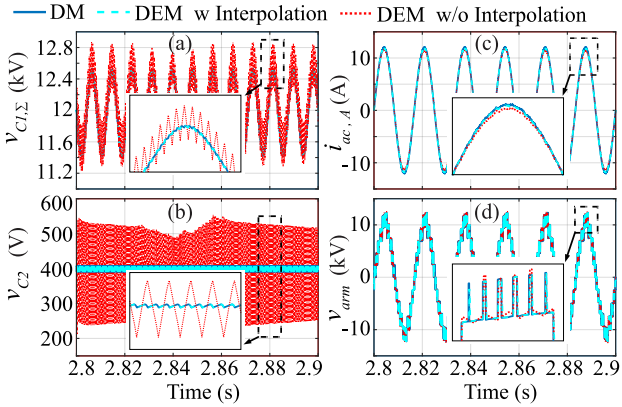

Fig. 9. Validation of switching interpolation technique. (a) Summation of MVDC-link capacitor voltages in Stage-I of phase A. (b) LVDC-link voltage in Stage-II. (c) Arm current of phase A. (d) Arm voltage of phase A.

Figs. 8 and 9 show that the results without interpolation are significantly distorted due to inaccurate detection of switching events. In contrast, the DEM with switching interpolation achieves high accuracy in both Stages I and II.

D. Validation of Simulation Efficiency

In this subsection, a CPU-only serial processing model of the SST is implemented to demonstrate the numerical efficiency gains of the proposed hybrid CPU-GPU DEM. The SST is simulated with different numbers of modules per phase. All models are simulated for 1s with a 5µs time step-size.

TABLE II
EXECUTION TIME COMPARISONS FOR SMALL-SCALE SST CONVERTERS

No. of Modules / Phase	DM	CPU-only	CPU-GPU	Speed-up $\left(\frac{\text{DM}}{\text{CPU}-\text{GPU}}\right)$	Speed-up $\left(\frac{CPU-only}{CPU-GPU}\right)$
5	152.04	13.16	8.42	18.05	1.56
10	489.20	18.52	8.81	55.52	2.10
20	1718.86	29.25	10.72	160.34	2.72
30	3689.00	39.61	12.54	294.17	3.15

Table II shows the comparison of execution times, measured in seconds, of the DM, CPU-only DEM, and the CPU-GPU DEM ranging from 5 to 30 modules per phase. The CPU-GPU DEM significantly outperforms both CPU-only DEM and DM model in terms of computational efficiency. For instance, with 30 modules per phase, the CPU-GPU DEM executes in only 12.54s, compared to 39.61s for the CPU-only DEM and 3689s for the DM. This corresponds to speed-up factors of 3.15 and 294.17 relative to the CPU-only and DM models, respectively.

Table III compares the execution times of larger converter scales. The execution time of the proposed CPU-GPU DEM remains nearly constant at around 16s. In contrast, the CPU-only execution time grows significantly, reaching 179.48s for 150 modules per phase. This results in speed-up factors up to 10.9, demonstrating the strong scalability and efficiency of the CPU-GPU implementation.

TABLE III
EXECUTION TIME COMPARISONS FOR LARGE-SCALE SST CONVERTERS

No. of Modules / Phase	CPU-only	CPU-GPU	Speed-up $\left(\frac{\text{CPU}-\text{only}}{\text{CPU}-\text{GPU}}\right)$
50	61.01	15.04	4.05
80	94.11	15.22	6.18
100	116.10	15.34	7.56
150	179.48	16.46	10.90

V. CONCLUSION

This paper proposes a fully decoupled DEM for the EMT simulation of SST. A CPU-GPU platform is developed for the parallel simulation of the SST DEM. The inherent parallelism of GPUs enables high efficiency compared with CPU-only implementation. Furthermore, a switching interpolation technique is incorporated to ensure the accuracy of the DEM for large simulation time steps. The accuracy and efficiency of the proposed DEM are validated through the comparison with Simulink DM model. The results show that the proposed CPU-GPU DEM achieves a 294-fold speed-up relative to a DM with 30 modules per phase. The large-scale models show that the parallel platform achieves 10-fold speed-up, compared to a CPU-only DEM implementation of the SST.

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