Enhanced Transient Control for Overprovisioned GFM-ESS under Asymmetric Current Limiting

Yafeng Tang, Li Sun, Qianhui Wei
School of Mechanical Engineering and Automation, *Harbin Institute of Technology, Shenzhen*, Shenzhen, China
Email: ctang763@foxmail.com, sunli2021@hit.edu.cn, wqh_200105@163.com

***Abstract*—Grid-forming energy storage systems (GFM-ESS) are increasingly deployed to enhance transient support and system resilience in high-renewable grids. When converters are overprovisioned (e.g., 3 p.u. converter capacity for a 1 p.u. ESS), asymmetric current limiting becomes essential to ensure strong AC-side reactive support while maintaining DC-side current safety. However, conventional circular limiters and voltage controllers often lead to converter locking in the current limiting control (CLC) mode or severe post-fault power oscillations. This paper proposes an enhanced transient control strategy for overprovisioned GFM-ESS under asymmetric limiting. First, an elliptical priority-based current limiter is adopted to satisfy asymmetric current constraints. Then, a back-calculation anti-windup (BCAW) voltage controller is employed to prevent post-fault locking. Finally, an adaptive power reference adjustment and a dual-feedforward damping control (VqFF + TEFF) are integrated to suppress active power oscillations and enable smooth transition from CLC to the constant voltage control (CVC). Simulations validate that the proposed control significantly improves fault ride-through capability and post-fault recovery stability of overprovisioned GFM converters.**

***Index Terms*—Grid-forming, energy storage system, asymmetric current limiting, anti-windup control, post-fault damping.**

I. Introduction

With the rapid growth of converter-interfaced renewable generation, future power systems are expected to operate under high penetration of power electronic converters. GFM converters, which emulate the electromechanical behavior of synchronous generators, have emerged as a key enabler for system stability, inertia support, and voltage regulation in such low-inertia networks [1], [2]. When coupled with ESS, GFM-ESS provide both fast frequency regulation and transient fault ride-through capability [3].

However, due to the voltage-source nature of GFM converters, their output voltage remains nearly constant during grid faults, which can cause excessive short-circuit current. Without proper current limiting, overcurrent protection may trigger converter disconnection, compromising transient stability [4], [5]. Therefore, effective current-limiting strategies are essential for GFM-ESS operation under grid faults.

Recent grid codes mandate GFM-ESS to provide strong reactive support, often up to three times the rated capacity during transients [8], [9]. To satisfy these requirements, overprovisioned converter capacity is adopted (e.g., a 1 p.u. ESS paired with a 3 p.u. converter). This creates asymmetric constraints—high reactive current on the AC side and limited active current on the DC side for battery safety—which conventional circular limiters cannot satisfy [10], [11]. Consequently, the mismatch between symmetric current limiting and asymmetric physical constraints leads to either excessive DC current or insufficient AC reactive support.

To address this issue, this paper proposes an elliptical priority-based current limiter for overprovisioned GFM-ESS, ensuring both AC-side support and DC-side protection. Furthermore, even with proper current limiting, the system may experience CLC mode locking or severe post-fault oscillations due to controller windup and weak damping [12], [13]. To overcome these challenges, an enhanced transient control scheme is developed, combining (1) a BCAW method voltage controller for desaturation, (2) adaptive active power reference adjustment for improved transient stability, and (3) post-fault damping control based on q-axis voltage and torque error feedforward (VqFF+TEFF).

The rest of this paper is organized as follows. Section II introduces the basic topology of GFM-ESS and a new kind of current limiter, Section III presents the anti-windup voltage control structure and analyzes its impact on anti-windup. Section IV introduces the transient stability enhancement and post-fault oscillation suppression strategy based on adaptive active power reference and VqFF+TEFF. Section V briefly discusses the case studies. Section VI concludes the paper.

II. GFM-ESS with Overprovisioned Converter

Fig. 1 shows a grid-connected GFM-ESS with a current limiter. The DC side of the GFM converter is connected to an energy storage battery with constant voltage U_{dc}. The AC side is connected to the PCC through an L–C filter (L_{f}, R_{f}, C_{f}) and line impedance (L_{g}, R_{g}). $U_{\mathrm{c}}^{\mathrm{abc}}$ and $I_{\mathrm{f}}^{\mathrm{abc}}$ denote the converter terminal voltage and filter inductor current, while $U_{\mathrm{p}}^{\mathrm{abc}}$ and $I_{\mathrm{g}}^{\mathrm{abc}}$ denote the point of common coupling (PCC) voltage and grid current. A dual-loop voltage–current control structure is adopted: $U_{\mathrm{ref}}^{\mathrm{dq}}$ is the PCC voltage reference, the voltage loop generates the current command $I_{\mathrm{cmd}}^{\mathrm{dq}}$, which is then limited to $I_{\mathrm{ref}}^{\mathrm{dq}}$ by the current limiter. The active synchronization loop uses virtual synchronous generator (VSG) control, whose dynamic equation is

$$J\frac{d^2\delta}{dt^2} = P_{\mathrm{ref}} - P - D\left(\omega - \omega_{\mathrm{N}}\right) \tag{1}$$

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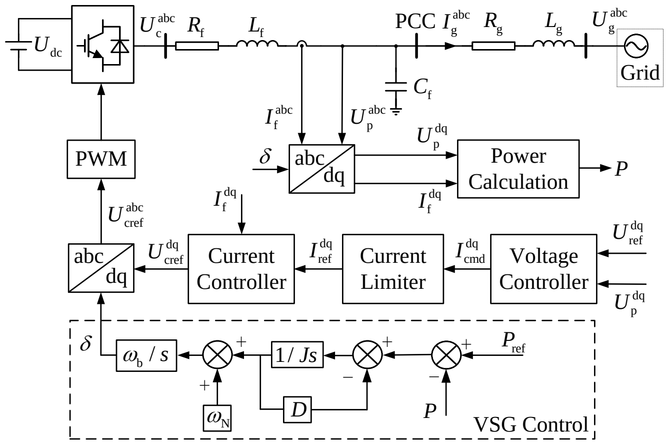

Figure 1. Topology and control structure of grid-connected GFM-ESS with current limiter.

where δ is the virtual power angle between the dq and abc frames, ω and ω_{N} are the VSG output and rated angular frequencies, P and P_{ref} are the converter active power and its reference, J and D are virtual inertia and damping coefficient. The current limiter in Fig. 1 restricts short-circuit current during grid-voltage sags. Since the current loop is much faster than the outer loop, the actual current can be assumed to track $I_{\mathrm{ref}}^{\mathrm{dq}}$ closely, so limiting the current reference from the voltage loop is sufficient for short-circuit current limiting.

However, the traditional circular limiter is not suitable for overprovisioned GFM-ESS. Its limiting boundary is a circle centered at the origin with radius $I_{\max}$. Setting $I_{\max} = 3$ p.u. cannot effectively restrict DC-side active current, while $I_{\max} = 1.2$ p.u. cannot provide enough AC-side reactive support. To meet the asymmetric constraint of "high reactive capability on the AC side, low allowable active overload on the DC side," an *elliptical current limiter* is adopted. It uses the semi-major and semi-minor axes to realize asymmetric current limiting while preserving a smooth boundary.

Circular current limiters generally operate in two modes [11]: magnitude limiting and priority-based limiting, as shown in Fig. 2(a)(b). Both constrain the current vector within the circular boundary, but differ in how they treat the angle ϕ_{I} between the limited current vector and the d-axis. In magnitude limiting mode, only the magnitude is scaled and the direction is preserved; in priority-based mode, both magnitude and angle are adjusted to a specified ϕ_{I}.

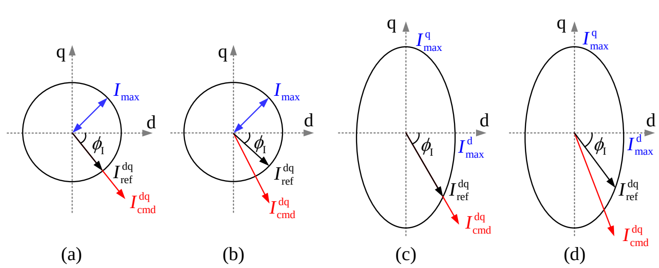

Figure 2. Illustration of circular and elliptical current limiters: (a) Circular magnitude limiter; (b) Circular priority-based limiter; (c) Elliptical magnitude limiter; (d) Elliptical priority-based limiter.

Following this idea, the elliptical limiter also has magnitude limiting and priority-based modes, as shown in Fig. 2(c)(d). In magnitude limiting mode, ϕ_{I} is not actively controlled and remains small during transients, which cannot fully exploit the overprovisioned reactive capability. Therefore, an *elliptical priority-based limiter* is proposed. Its boundary is defined by

$$\left(\frac{I_{\mathrm{f}}^{\mathrm{d}}}{I_{\max}^{\mathrm{d}}}\right)^2 + \left(\frac{I_{\mathrm{f}}^{\mathrm{q}}}{I_{\max}^{\mathrm{q}}}\right)^2 = 1 \tag{2}$$

where $I_{\max}^{\mathrm{d}} = 1.2$ p.u. and $I_{\max}^{\mathrm{q}} = 3.0$ p.u.. The semi-axis $I_{\max}^{\mathrm{d}}$ protects the DC-side battery, while $I_{\max}^{\mathrm{q}}$ exploits the AC-side reactive capacity. The corresponding equivalent current amplitude on the ellipse is

$$I_{\max} = \frac{I_{\max}^{\mathrm{d}} I_{\max}^{\mathrm{q}}}{\sqrt{(I_{\max}^{\mathrm{d}} \sin\phi_{\mathrm{I}})^2 + (I_{\max}^{\mathrm{q}} \cos\phi_{\mathrm{I}})^2}} \tag{3}$$

The elliptical priority-based limiter not only constrains the current magnitude to the elliptical boundary $I_{\max}$, but also forces the current angle to a specified ϕ_{I}, which is a tunable parameter. A larger ϕ_{I} allows the inverter to provide more reactive current. Its mathematical formulation is

$$\begin{cases} \left.\begin{aligned} I_{\mathrm{ref}}^{\mathrm{d}} &= I_{\max}\cos\phi_{\mathrm{I}} \\ I_{\mathrm{ref}}^{\mathrm{q}} &= I_{\max}\sin\phi_{\mathrm{I}} \end{aligned}\right\} & \text{if } \alpha > 1, \\ I_{\mathrm{ref}}^{\mathrm{dq}} = I_{\mathrm{cmd}}^{\mathrm{dq}}, & \text{otherwise.} \end{cases} \tag{4}$$

where $\alpha = (I_{\mathrm{cmd}}^{\mathrm{d}}/I_{\max}^{\mathrm{d}})^2 + (I_{\mathrm{cmd}}^{\mathrm{q}}/I_{\max}^{\mathrm{q}})^2$. If $\alpha > 1$, the limiter is activated. By choosing ϕ_{I}, a smooth compromise between battery protection and reactive support can be achieved.

III. Anti-Windup and Smooth Recovery Control

A. Motivation and Problem Description

Similar to circular-limit GFM converters, those equipped with an elliptical limiter may become trapped in the CLC mode after fault clearance. As reported in [12], the recovery condition for the CVC mode requires $\left|\mathbf{I}_{\mathrm{f}}^{\mathrm{dq}}(\delta)\right| < I_{\max}$ and $\mathbf{I}_{\mathrm{cmd}}^{\mathrm{dq}}$ within the limiter boundary. The post-fault recovery behavior largely depends on the voltage controller structure and its anti-windup design. Three typical configurations are compared in Fig. 3, including traditional PI controller using the clamping anti-windup (CAW) method, direct PI controller using the CAW method, and direct PI controller using back-calculation anti-windup (BCAW) method.

B. Direct PI Controller with CAW

Fig. 3(a) depicts the traditional PI voltage controller using CAW, where k_{pv} and k_{iv} denote proportional and integral gains. The transition between CVC and CLC is determined by factor d: when $\alpha \le 1$, the integrator is active ($d = 1$); otherwise, it is frozen ($d = 0$). Here, $\alpha > 1$ denotes current-limiter engagement (actuator saturation), which triggers CAW. In the traditional PI voltage controller, a grid current feed-forward term is introduced to ensure that the PI controller output remains zero during normal operation. As noted in [13],

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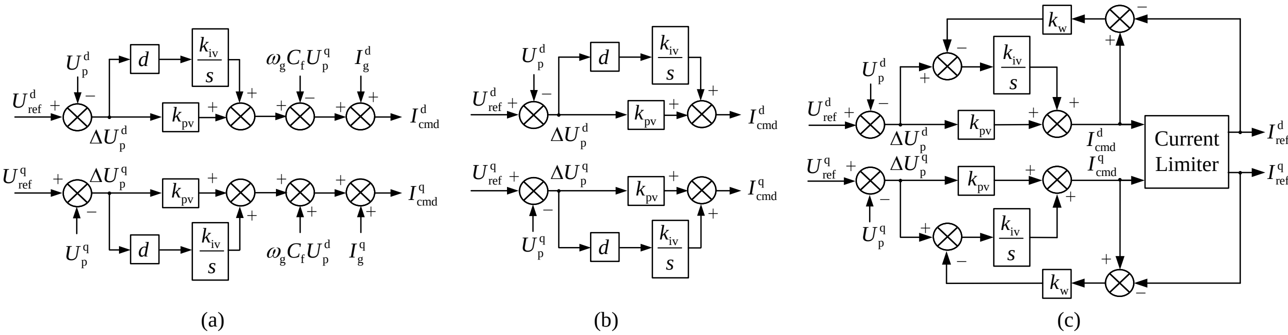

Figure 3. Voltage control loops with different anti-windup strategies and controllers: (a) Traditional PI controller using the CAW method; (b) Direct PI controller using the CAW method; (c) Direct PI controller using the BCAW method.

under CLC, the feedforward term equals $I_{\max}$, which makes it difficult for the GFM converter to recover from CLC to CVC.

To simplify the structure, a direct PI controller without grid current feedforward is adopted (see Fig. 3(b)). The law is (5), where $\Delta U_{\mathrm{p}}^{\mathrm{dq}}$ are PCC voltage errors.

$$\begin{aligned} I_{\mathrm{cmd}}^{\mathrm{d}} &= k_{\mathrm{pv}}\Delta U_{\mathrm{p}}^{\mathrm{d}} + d\cdot\frac{k_{\mathrm{iv}}}{s}\Delta U_{\mathrm{p}}^{\mathrm{d}},\\ I_{\mathrm{cmd}}^{\mathrm{q}} &= k_{\mathrm{pv}}\Delta U_{\mathrm{p}}^{\mathrm{q}} + d\cdot\frac{k_{\mathrm{iv}}}{s}\Delta U_{\mathrm{p}}^{\mathrm{q}}. \end{aligned} \tag{5}$$

During faults, the current quickly exceeds the limiter boundary, freezing the integrator at $x_{\mathrm{freeze}}^{\mathrm{dq}}$. When the grid voltage recovers, the voltage error decreases, but the large integral term k_{pv} may cause re-saturation. Consequently, the CAW-based direct PI controller can still experience post-fault locking.

C. Direct PI Controller with BCAW

To overcome this problem, a direct PI controller with BCAW method is proposed, as illustrated in Fig. 3(c). The BCAW method introduces a feedback term proportional to the current difference $(\mathbf{I}_{\mathrm{cmd}}^{\mathrm{dq}} - \mathbf{I}_{\mathrm{ref}}^{\mathrm{dq}})$ to accelerate desaturation. The control law is (6), where k_{w} is the back-calculation gain.

$$\begin{aligned} I_{\mathrm{cmd}}^{\mathrm{d}} &= k_{\mathrm{pv}}\Delta U_{\mathrm{p}}^{\mathrm{d}} + \frac{k_{\mathrm{iv}}}{s}\left[\Delta U_{\mathrm{p}}^{\mathrm{d}} - k_{\mathrm{w}}(I_{\mathrm{cmd}}^{\mathrm{d}} - I_{\mathrm{ref}}^{\mathrm{d}})\right],\\ I_{\mathrm{cmd}}^{\mathrm{q}} &= k_{\mathrm{pv}}\Delta U_{\mathrm{p}}^{\mathrm{q}} + \frac{k_{\mathrm{iv}}}{s}\left[\Delta U_{\mathrm{p}}^{\mathrm{q}} - k_{\mathrm{w}}(I_{\mathrm{cmd}}^{\mathrm{q}} - I_{\mathrm{ref}}^{\mathrm{q}})\right]. \end{aligned} \tag{6}$$

By setting $k_{\mathrm{w}} = 1/k_{\mathrm{pv}}$ and considering $k_{\mathrm{iv}} \gg k_{\mathrm{pv}}$, the commanded current can be approximated as

$$I_{\mathrm{cmd}}^{\mathrm{dq}} \approx k_{\mathrm{pv}}\Delta U_{\mathrm{p}}^{\mathrm{dq}} + I_{\mathrm{ref}}^{\mathrm{dq}}. \tag{7}$$

This relationship ensures $\mathbf{I}_{\mathrm{cmd}}^{\mathrm{dq}} \approx \mathbf{I}_{\mathrm{ref}}^{\mathrm{dq}}$ during faults, resulting in shallower saturation and faster recovery. After fault clearance, decreasing voltage errors drive desaturation and enable a smooth transition from CLC back to CVC. Compared with CAW, the BCAW controller effectively prevents integrator windup and avoids post-fault locking, thereby ensuring stable restoration of voltage control.

IV. Transient Stability Enhancement and Post-Fault Oscillation Suppression

To enhance fault ride-through performance, the coordinated control scheme in Fig. 4 is adopted. Transient stability is improved by reducing the active power reference during the fault, while post-fault oscillations are suppressed by additional damping terms and appropriate mode switching.

A. Adaptive Active Power Reference During Fault

As shown in the red dashed box of Fig. 4(a), the active power reference is adaptively adjusted according to the PCC voltage magnitude U_{pmag}: $P_{\mathrm{ref,adp}} = P_{\mathrm{ref}} - k_{\mathrm{m}}(U_{\mathrm{N}} - U_{\mathrm{pmag}})$, where U_{N} is the rated PCC voltage and $k_{\mathrm{m}} = P_{\mathrm{N}}/U_{\mathrm{N}}$ is a normalization factor.Here, $U_{\mathrm{pmag}} = \sqrt{(U_{\mathrm{p}}^{\mathrm{d}})^2 + (U_{\mathrm{p}}^{\mathrm{q}})^2}$ denotes the PCC voltage magnitude in the synchronous reference frame (RMS value), which equals U_{N} in steady state and decreases during faults [13], [14]. This adjustment makes active power and voltage decrease approximately proportionally, alleviating power imbalance and improving transient stability.

B. Post-Fault Damping with VqFF and TEFF

After fault clearance, the system may suffer from active power oscillations and even power backflow [15], especially under current limiting and weak damping. To improve post-fault dynamics, the strategy in the green dashed box of Fig. 4(a) is adopted, combining q-axis voltage feedforward (VqFF) and torque error feedforward (TEFF) [13].

(1) VqFF: When the grid voltage recovers from the fault value to the rated value, the q-axis voltage $U_{\mathrm{p}}^{\mathrm{q}}$ experiences a step change. VqFF converts this into a frequency step $\Delta\omega_{\mathrm{VqFF}} = k_{\mathrm{VqFF}}\,\Delta U_{\mathrm{p}}^{\mathrm{q}}$, which is equivalent to injecting additional kinetic energy. This prevents the converter from settling at the incorrect equilibrium introduced by the limiter and accelerates the desaturation process.

(2) TEFF: The active power deviation ΔP is fed into the frequency loop through k_{TEFF} to reshape the rotor motion equation and increase the effective damping, thereby suppressing power-angle overshoot and post-fault oscillations.

C. Mode-Switching Logic

The fault process is divided into four states (normal, fault, post-fault 1, and post-fault 2), as shown in Fig. 4(b). The post-fault control (VqFF+TEFF) is activated during the transition from fault to post-fault 1 and smoothly disabled thereafter.

(1) Trigger logic: U_{pmag} with hysteresis thresholds is used for mode detection. When $U_{\mathrm{pmag}} \leq 0.9$ p.u., the system enters the fault state; when $U_{\mathrm{pmag}} \geq 0.85$ p.u. after fault clearance,

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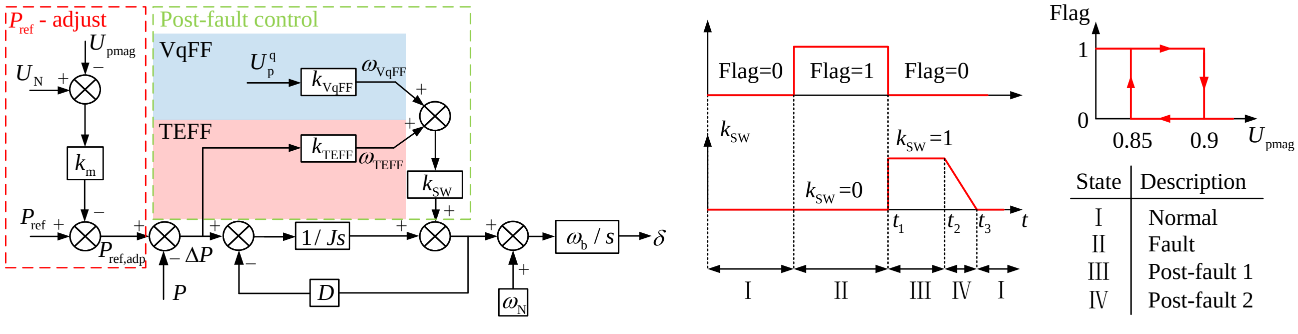

Figure 4. Transient stability enhancement and post-fault active power oscillation suppression strategy: (a) Control structure; (b) Control logic.

post-fault recovery is detected and $k_{\rm sw}$ is set to 1 to activate VqFF and TEFF.

(2) Exit mechanism: Two conditions must hold for a certain time to ensure a safe exit: i) $\Delta P < 1$ p.u., indicating that active power is close to its rated value; ii) the current limiter is inactive and the converter operates stably in CVC mode. If both conditions persist for 100 ms, $k_{\rm sw}$ is ramped down to zero with a slope of -2 p.u./s, so that the VqFF and TEFF feedforward terms are smoothly removed. This avoids control signal jumps and allows the system to return to the conventional GFM mode without exciting new oscillations. If a subsequent fault is detected during the post-fault recovery interval (e.g., due to high-speed reclosing), the logic immediately resets $k_{\rm sw}$ and returns the system to the fault state, ensuring correct reactivation of the post-fault control without adverse interaction.

V. Simulation Results

A GFM-ESS model shown in Fig. 1 was built in Matlab/Simulink. The system is rated at 10 kVA/380 V, with a 3 p.u. overprovisioned converter. The PCC voltage is regulated by an outer PI loop $(k_{\rm pv}, k_{\rm iv})$ and an inner current loop $(k_{\rm pi}, k_{\rm ii})$. The elliptical limiter limits $I^{\rm d}_{\rm max} = 1.2$ p.u. and $I^{\rm q}_{\rm max} = 3$ p.u.. Other parameters are summarized in Table I. A voltage fault is applied at $t = 0.5$ s and cleared after t_c, and simulation cases are conducted for comparison.

Table I
Simulation Parameters

Variable	Value	Variable	Value
$U_{\rm dc}$	1000 V	$\phi_{\rm I}$	-1.3 rad
$L_{\rm g}$	9.2 mH (0.2 p.u.)	$k_{\rm pv}$	0.02 p.u.
$L_{\rm f}$	6.9 mH (0.15 p.u.)	$k_{\rm iv}$	500 p.u.
$R_{\rm f}$	0.216 Ω (0.015 p.u.)	$k_{\rm pi}$	3 p.u.
$C_{\rm f}$	13.2 μF (0.06 p.u.)	$k_{\rm ii}$	150 p.u.
$\omega_{\rm N}$	314.16 rad/s (1 p.u.)	$k_{\rm w}$	50 p.u.
$U_{\rm g}$ (L–L rms)	380 V (1 p.u.)	$I^{\rm d}_{\rm max}$	1.2 p.u.
$P_{\rm ref}$	10 kW (1 p.u.)	$I^{\rm q}_{\rm max}$	3.0 p.u.
J	8 kg·m^2	$k_{\rm VqFF}$	4 p.u.
D	60 W·s/rad	$k_{\rm TEFF}$	0.2 p.u.

A. Case 1: System with the CAW Method Voltage Controller

The converter adopts a direct PI voltage controller with the CAW method. Fig. 5(a) shows system responses under zero-voltage fault condition ($U_{\rm gF} = 0$ p.u.), where the critical clearing time lies between 430 ms and 440 ms. Fig. 5(b) shows the response under a voltage sag ($U_{\rm gF} = 0.4$ p.u.), in which power angle stability is maintained during the fault. In both cases, the system remains locked in CLC after fault clearance and fails to recover to CVC.

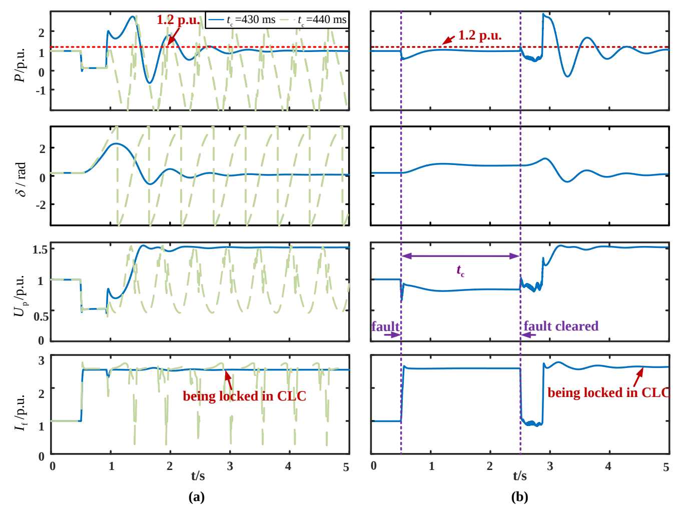

Figure 5. Simulation results with the CAW method voltage loop: (a) zero-voltage fault condition; (b) voltage sag ($U_{\rm gF} = 0.4$ p.u.).

B. Case 2: System with the BCAW Method Voltage Controller

The voltage controller employs the proposed BCAW direct PI control. As shown in Fig. 6(a) and (b), the system successfully exits the CLC mode and recovers to CVC after fault clearance under both zero-voltage fault and voltage sag conditions. However, noticeable active power oscillations occur immediately after fault clearing, which may cause temporary DC-side power overshoot.

C. Case 3: System with BCAW Voltage Controller and Post-Fault Damping.

In this case, the converter adopts the full coordinated control combining the BCAW method, adaptive power reference adjustment, and post-fault damping via VqFF and TEFF

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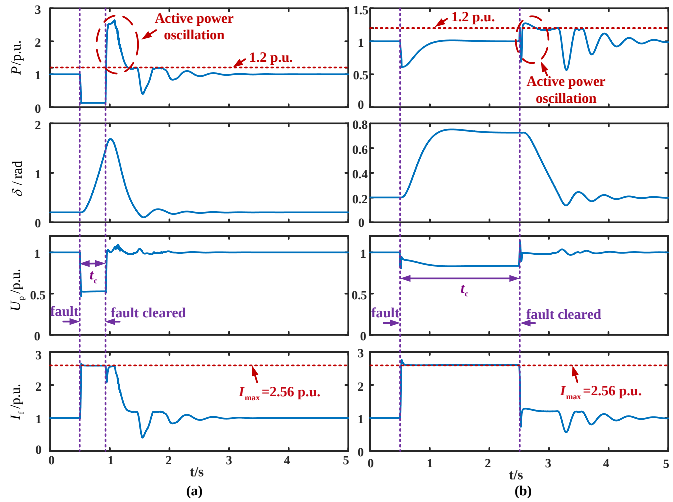

Figure 6. Simulation results with the BCAW method voltage loop: (a) zero-voltage fault condition; (b) voltage sag ($U_{\mathrm{gF}} = 0.4$ p.u.).

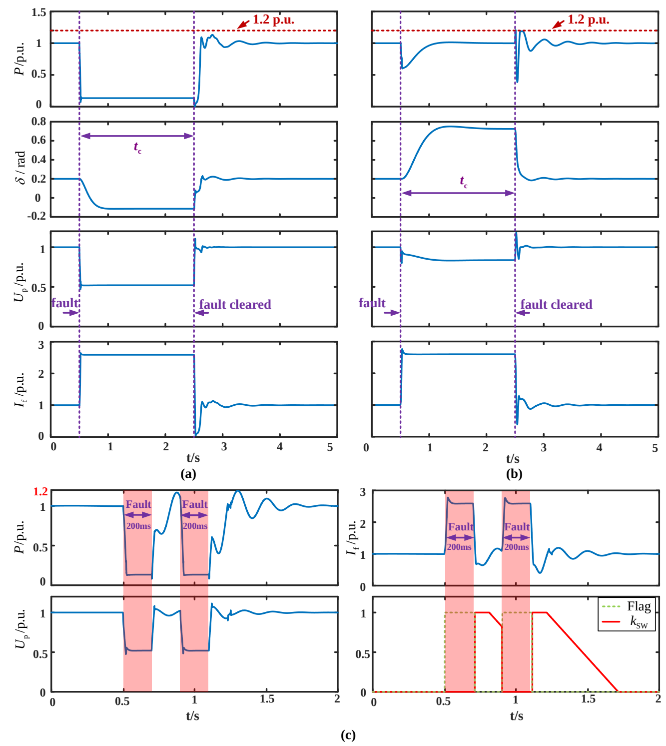

Figure 7. Simulation results with the BCAW voltage controller and additional transient control: (a) zero-voltage fault condition; (b) voltage sag ($U_{\mathrm{gF}} = 0.4$ p.u.); (c) HSR under zero-voltage fault condition.

feedforward. Fig. 7(a) and (b) show system responses under zero-voltage fault condition ($U_{\mathrm{gF}} = 0$ p.u.) and voltage sag ($U_{\mathrm{gF}} = 0.4$ p.u.), both with $t_{\mathrm{c}} = 2$ s. After fault clearance, the converter smoothly exits the CLC mode and resumes CVC operation. Active power remains stable without overshoot, confirming smooth and oscillation-free post-fault recovery. To further verify robustness against high-speed reclosing (HSR), Fig. 7(c) shows system responses under repeated faults occurring within the post-fault recovery window, where k_{sw} is immediately reset upon fault re-detection, ensuring stable operation without control conflict.

VI. Conclusion

This paper investigated a coordinated transient control scheme for overprovisioned GFM-ESS under asymmetric current limiting. By integrating an elliptical priority-based current limiter, a BCAW-based voltage controller, and adaptive post-fault damping, the proposed method enables stable fault ride-through and smooth recovery from CLC to CVC while maintaining DC-side safety and AC-side reactive capability. The results demonstrate a practical control solution for enhancing transient resilience of grid-forming energy storage systems in high-renewable power grids.

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