PHIL Interface Evaluation in Data Center Application

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***Abstract*—Data centers are experiencing a surge in power consumption due to the increasing complexity of artificial intelligence (AI) models. The fluctuating power demand associated with AI training workloads can introduce sub-synchronous harmonics (SSHs), potentially destabilizing the utility grid. Power hardware-in-the-loop (PHIL) simulation offers a promising approach to study these harmonics and assess grid compliance. However, PHIL simulation itself might cause instability and inaccuracies, mainly due to PHIL interface where software and hardware are connected. This paper evaluates various PHIL interfaces in the data center application to study SSHs and fault scenarios . A real-time simulation of a data center is conducted using the RTDS platform, and the grid power spectrum is analyzed via Fast Fourier Transform (FFT). Based on the results, recommendations are provided for selecting the most appropriate PHIL interface for data center applications.**

***Index Terms*—Data center, PHIL, Artificial Intelligence, real-time simulation.**

I. Introduction

Data centers have become significant contributors to grid dynamics due to their large and fluctuating power demand, driven by the exponential growth in artificial intelligence (AI) model complexity and the corresponding increase in computational demand. Early models like AlexNet [1], with approximately 60 million parameters, could be trained on a single graphics processing unit (GPU). In contrast, foundation models often contain billions of parameters and require tens of thousands of GPUs operating in parallel [2]. These GPUs alternate between computation and communication phases during training, resulting in significant power fluctuations that propagate to the grid [3]. Such fluctuations can generate sub-synchronous harmonics (SSHs), which may excite torsional resonances in generator shafts and trigger inter-area oscillations [4]. Understanding and mitigating these effects is essential to ensure grid stability and regulatory compliance.

Power hardware-in-the-loop (PHIL) simulation is a practical method for analyzing SSHs in data centers. It enables the integration of actual hardware, referred to as the device under test (DUT), with a simulated rest of system (ROS) running on a real-time simulator. The DUT and ROS are connected via a power amplifier interface, which introduces non-idealities such as time delays, signal distortion, and bandwidth limitations. These factors can compromise simulation accuracy and stability [5].

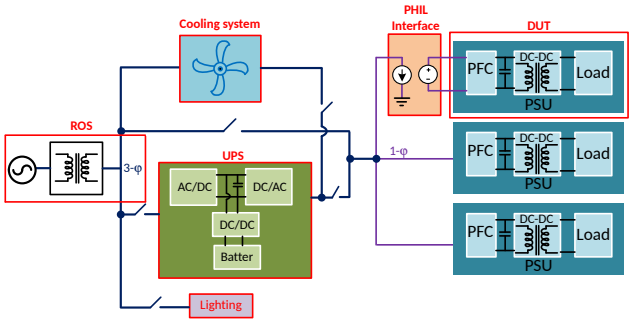

Fig. 1. System configuration of a data center with PHIL interface.

Several PHIL interface techniques have been proposed, including the ideal transformer model (ITM), transmission line model (TLM), time-variant first-order approximation (TFA), and Embedded interfaces [6]–[9]. Prior research has explored the stability of these methods using analytical derivation of loop transfer function or impedance measurement [6]. However, their performance in data center applications has not yet been investigated, which is the focus of this paper. To address this gap, a real-time simulation of a data center, shown in Fig. 1, was developed to compare the ITM and Embedded interfaces, representing conventional and advanced PHIL techniques, respectively, against a reference case without PHIL interface. The evaluation focuses on:

- Steady-state and controller performance
- Dynamic load and resulting SSHs via Fast Fourier Transform (FFT)
- Fault response
- Frequency response
- Recommendations for selecting a suitable PHIL interface

II. PHIL Interface

ROS and DUT should be interfaced appropriately to ensure stable and accurate PHIL simulation. The ITM is one of the most conventional and straightforward PHIL interface methods [6], shown in Fig. 2(a). Its stability depends on the impedance ratio between ROS and DUT. In contrast, TLM interface offers inherent stability regardless of the impedance ratio between ROS and DUT [7]. Moreover, TLM can be integrated into existing transmission lines within the ROS. However,

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its implementation requires a physical resistor at the power amplifier to emulate the line's characteristic impedance. This resistor can lead to increased power consumption and reduced output voltage range. The effect of the physical resistor can be emulated in FPGA at the cost of more computational resources [7].

To address loop delay in PHIL simulation, prediction-based interfaces have been introduced. These methods estimate DUT behavior using historical data. A conceptual diagram of this approach is shown in Fig. 2(b) and (c), where voltage v_R is computed based on ROS and DUT model. One such method is the TFA interface, which approximates the DUT as a first-order linear system [8]. For example, DUT can be modeled by an RL circuit, approximately, which is formulated by (1). To determine the coefficients α and β, a system of equations is formed using historical data. However, solving these equations often involves matrix inversion, which can be ill-conditioned and numerically unstable.

$$i_2(k) \approx \alpha \times v_D(k-1) + \beta \times i_2(k-1) = G_{eq} \times v_D(k-1) + i_{eq} \tag{1}$$

More advanced prediction algorithms aim for exact modeling of the DUT. One example is the Embedded PHIL interface which uses quasi multi-rate (QMR) integration to model a single-phase inverter with an LCL filter, shown in Fig. 2(c) [9]. In this method, passive components such as inductors and capacitors are represented using admittance and current source, a standard approach in the electromagnetic transient (EMT) simulation. However, the admittance and the current source are determined using QMR integration rather than trapezoidal integration. In fact, QMR method allows integration over a time span equal to the PHIL loop delay, effectively compensating the PHIL loop delay. Nevertheless, this technique requires impedance measurements of the DUT to estimate the loop delay.

III. Data Center

A. Operation Principle

A data center operates under three distinct modes depending on the grid voltage level (v_G), as outlined below [10]:

- Normal eco mode ($0.9 < v_G < 1.1$): In this mode, server loads are directly powered by the grid. The uninterruptible power supply (UPS) operates at light load, primarily to facilitate smooth transitions and accelerate the startup procedure.
- Double conversion mode ($0.7 < v_G < 0.9$): When the grid voltage drops below the acceptable range for the data center but remains within the UPS operating limits, the UPS supplies power to the server loads.
- Battery mode ($v_G < 0.7$): In this mode, the UPS disconnects from the grid, and the backup battery system takes over to supply power to the server loads. This mode is typically triggered during severe grid disturbances or outages.

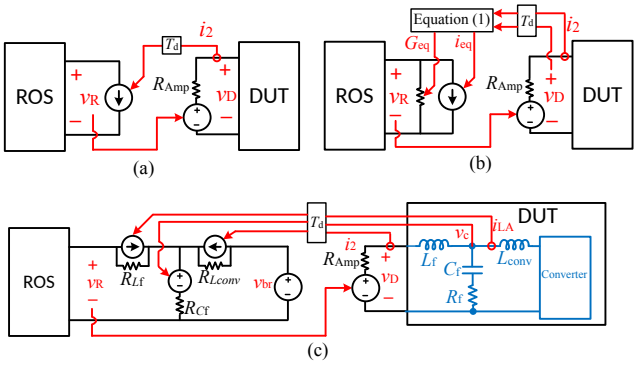

Fig. 2. PHIL simulation with (a) ITM interface (b) TFA interface (c) Embedded interface.

TABLE I
Mode frequencies of SSOs in the power system.

Frequency range	Oscillation source
0.01 – 0.15 Hz	Governor, plant controller, or automatic generation control
0.15 – 1.00 Hz	Electromechanical inter-area and some local plant oscillations
1.00 – 5.00 Hz	Local generator control oscillations, excitation controls, DC circuit controls
5.00 – 50.00 Hz	High (sub-synchronous) frequency torsional, DC controls, inverter-based generation controls, sub-synchronous interactions

B. Training Phases

Large-scale AI training typically follows synchronous parallelism, where each iteration consists of two distinct phases:

- Computation Phase: Each GPU independently processes a mini-batch of data, performing forward and backward passes to generate predictions and compute gradients of a loss function. This phase is highly power-intensive, with GPUs operating near their thermal design power (TDP) due to heavy utilization of tensor cores.
- Communication Phase: After gradients are computed, GPUs synchronize to aggregate and share the gradients, usually through all-reduce operations. During this phase, GPU utilization drops significantly, resulting in sharp reductions in power consumption.

C. Power Frequency Spectrum

Data centers have a fluctuating power demand due to switching between the computation and communication phases, frequently. This power profile emits SSHs in the range of 0.1 Hz to 20 Hz, as reported in [3]. Therefore, the power frequency spectrum of data centers might excite various sub-synchronous oscillations (SSOs) in the power system. Typical frequencies of SSOs in the power system that might be affected by data centers are summarized in Table I [11].

IV. PHIL Interface Evaluation

A. Methodology

To evaluate the performance of different PHIL interfaces, a comprehensive real-time simulation was conducted. The sim-

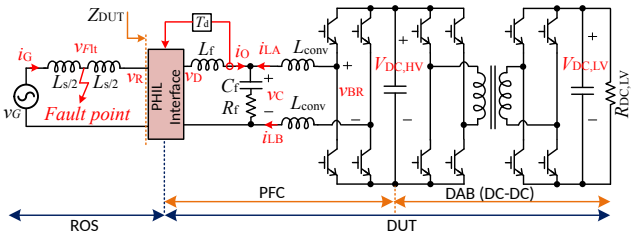

Fig. 3. Data center configuration in normal eco mode with PHIL interface.

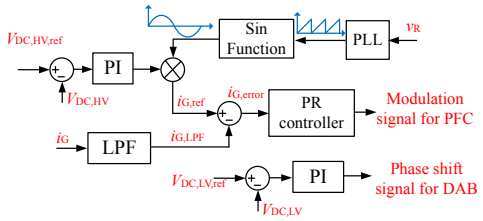

Fig. 4. Controller block diagram.

ulation encompassed the entire system, including ROS, DUT, and the PHIL interface, within a single simulation platform. A substep simulation environment with timestep (ΔT) of 4.16 μs is used. The study focused on a data center operating in the normal eco mode, where the utility grid and line impedance were modeled as ROS, and power supply unit (PSU) was designated as DUT, shown in Fig. 3. DUT comprises a single-phase power factor correction (PFC) converter with an LCL filter and a dual active bridge (DAB) converter as DC-DC stage, shown in Fig. 3. The PFC converter was controlled using proportional resonant (PR) controller, and DAB used a phase shift modulation controller, as shown in Fig. 4. Three cases were evaluated: a reference case (no PHIL interface), the ITM interface, and the Embedded interface. To emulate real-world conditions, non-idealities such as communication and amplifier delays were introduced by applying a lump-sum delay (T_d) to the feedback signals from DUT to ROS. The loop delay was measured by the method introduced in [9] using phase response of Z_{DUT}. The simulation parameters were listed in Table II.

TABLE II
SIMULATION PARAMETERS.

Parameter	Value	Value	Value
L_{conv}	567.2 μH	v_G	220 Vrms
L_s =L_f	2.0 mH	S_G	11 kVA
C_f	4.7 mF	$v_{DC,HV}$	350 V
R_f	3.6 Ω	$v_{DC,LV}$	48 V
R_{Amp}	0.2 Ω	f_{grid} = $f_{res,PR}$	50.0 Hz
Loop delay	20.94 ms	f_{sw}	10.0 kHz

B. Evaluation with Constant Load

The system was first tested under a constant load using the ITM interface. As shown in Fig. 5, the terminal voltages (v_R and v_D) matched closely, and the PR controller achieved

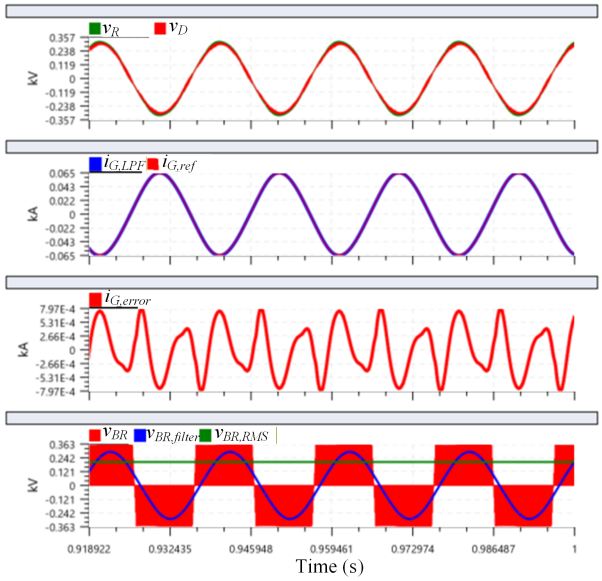

Fig. 5. Simulation results verifying ITM interface and the controller with a constant load.

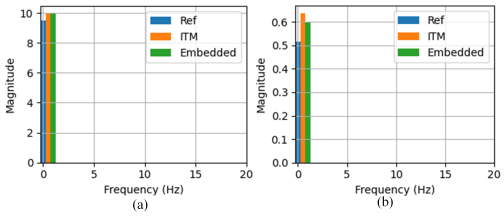

Fig. 6. FFT of (a) active power and (b) reactive power when the constant load is applied.

steady-state operation. The PFC converter operated with a unipolar modulation scheme, confirmed by the high-frequency waveform of v_{BR}. To highlight the differences between the ITM and Embedded interfaces compared to the reference case, FFT analysis was conducted on active power (P_G) and reactive power (Q_G), as shown in Fig. 6. FFT errors of the ITM and Embedded interfaces were calculated by the equations (2) and (3), listed in Table III, revealing that both of them have almost the same P_G error, mainly caused by amplifier resistor (R_{Amp}). However, the Embedded interface yielded more accurate results in terms of Q_G.

TABLE III
PHIL SIMULATION ACCURACY WITH A CONSTANT LOAD.

	$P_{G,error}$	$Q_{G,error}$
ITM interface	3.86 %	1.102 %
Embedded interface	3.99 %	0.774%

C. Evaluation with Dynamic Load

To mimic real data center behavior, a dynamic load was applied to simulate alternating computation and communication phases. The time-domain simulation waveforms of the three cases are shown in Fig. 7. It reveals slight mismatch in P_G

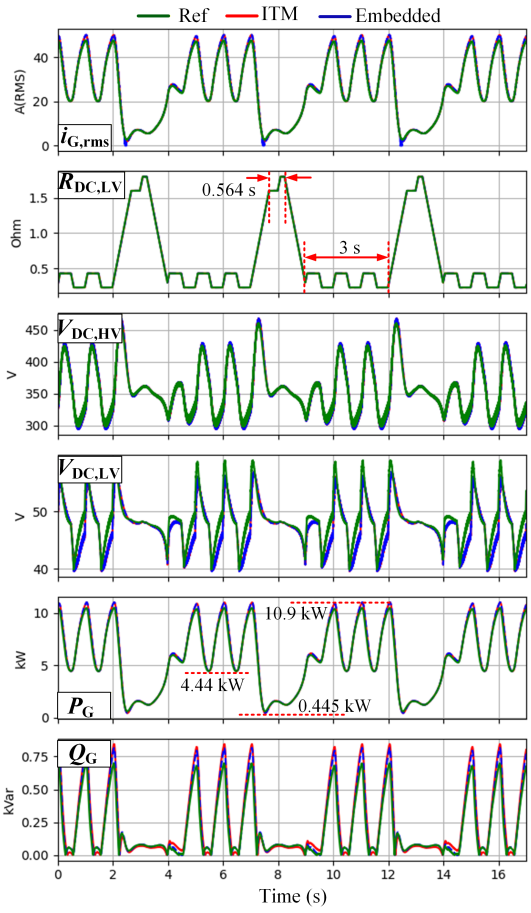

Fig. 7. Simulation results with the dynamic load.

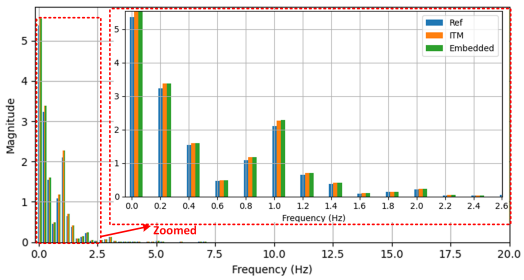

Fig. 8. FFT of active power when the dynamic load is applied.

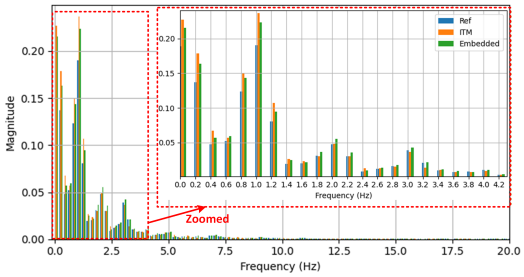

Fig. 9. FFT of reactive power when the dynamic load is applied.

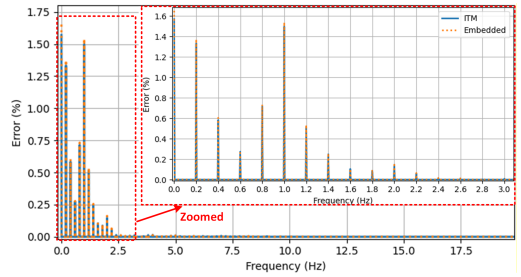

Fig. 10. FFT error of active power when the dynamic load is applied.

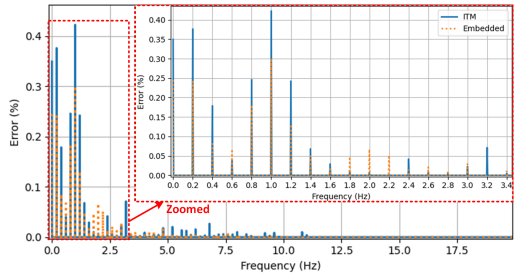

Fig. 11. FFT error of reactive power when the dynamic load is applied.

and noticeable mismatch in Q_G. To further investigate these discrepancies, FFT analysis was performed on both P_G and Q_G, shown in Fig. 8 and Fig. 9, with the corresponding errors illustrated in Fig. 10 and Fig. 11, calculated by equations (2) and (3), respectively.

$$P_{G,error} = \frac{P_{G,ITM} - P_{G,ref}}{S_G} \tag{2}$$

$$Q_{G,error} = \frac{Q_{G,ITM} - Q_{G,ref}}{S_G} \tag{3}$$

For P_G , the Embedded interface exhibited an FFT error of up to 1.65%, while the ITM interface showed a slightly lower error of up to 1.57%. For Q_G, the Embedded interface showed higher accuracy compared to the ITM interface, although there were a few SSHs where the ITM performed better.

D. Fault Evaluation

A phase-to-ground fault was introduced at 130° of the voltage waveform for a duration of 0.1 seconds. Fig. 12(a) shows the voltage at the fault point (v_{Flt}), while Fig. 12(b) displays the grid current response. The simulated fault using the Embedded interface matches the reference case. However, the ITM interface showed oscillatory behaviour and a high voltage spike which is not expected according to the reference case. These discrepancies are attributed to uncompensated loop delay inherent in the ITM interface.

E. Evaluation Based on Impedance Measurement

The DUT impedance (Z_{DUT}) was measured from the point shown in Fig. 3 which includes PHIL interface as well. In SSHs frequency range, i.e. less than 20 Hz, the ITM and Embedded interfaces match with the reference, shown in Fig. 13. The phase of Z_{DUT} in the ITM interface starts to diverge at

400 Hz while the phase of of Z_{DUT} in the Embedded interface matches with the reference at high frequencies, due to the delay compensation. Moreover, the magnitude of Z_{DUT} in the Embedded interface starts to diverge at 2.7 kHz, shown in Fig. 13.

F. Recommendations for Choosing a PHIL Interface

Selecting an appropriate PHIL interface for data center applications depends on the specific objectives of the simulation. Based on the evaluation results, the following recommendations are provided:

- Controller and power flow verification: The ITM interface is generally sufficient for verifying controller performance and basic power flow behavior. However, its stability is highly sensitive to the impedance ratio between the ROS and DUT and should be carefully assessed during implementation.
- SSH analysis and regulatory compliance: For evaluating SSHs in P_G, the ITM interface is preferred due to its simplicity and relatively high accuracy. Nonetheless, a margin should be considered to account for potential errors. In contrast, for Q_G, the Embedded interface has higher accuracy compared to the ITM interface. However, depending on the application, Q_G error of the ITM interface might be acceptable.
- Fault evaluation: If detailed high-frequency fault dynamics are of interest, advanced methods such as the Embedded interface are recommended. Otherwise, the ITM interface can provide only a rough approximation of fault behavior.

V. Conclusion

This paper evaluated PHIL interfaces for simulating SSHs and fault scenarios in data center applications. Results showed that the ITM interface is sufficient for verifying controller performance, basic power flow, and SSHs. While more advanced methods like the Embedded interface have higher accuracy in fault simulations. Future works can focus to improve the high-frequency response of the Embedded interface.

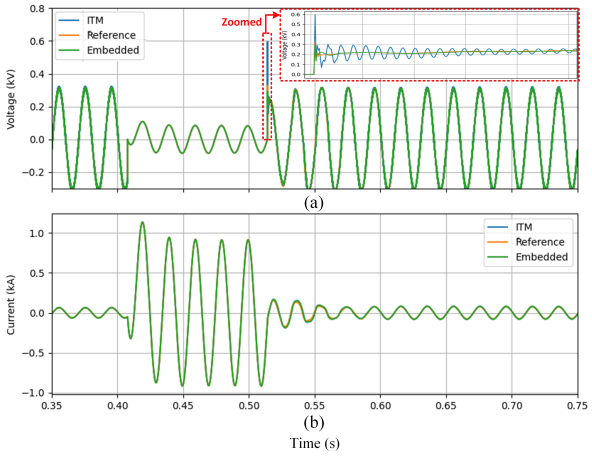

Fig. 12. PHIL interfaces performance under fault. (a) fault voltage (v_{Flt}) (b) grid current (i_G).

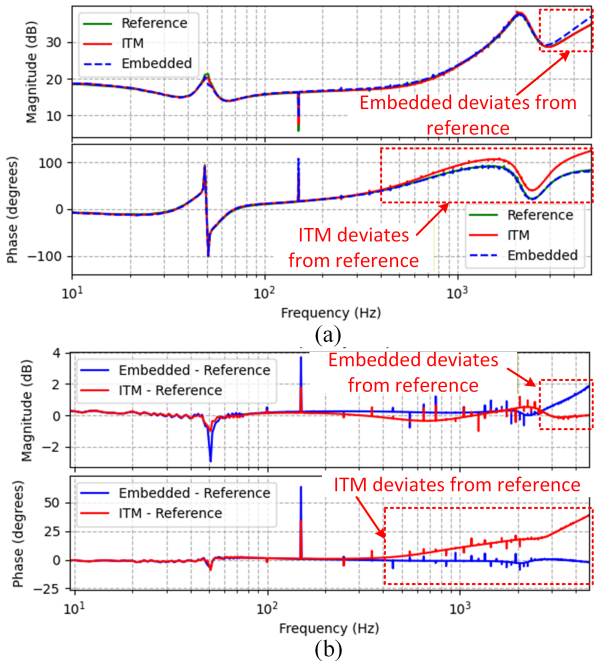

Fig. 13. Comparison of (a) impedance measurements (b) error.

References

[1] A. Krizhevsky, I. Sutskever, and G. E. Hinton, "Imagenet classification with deep convolutional neural networks," in *Advances in Neural Information Processing Systems*, F. Pereira, C. Burges, L. Bottou, and K. Weinberger, Eds., vol. 25. Curran Associates, Inc., 2012.

[2] A. Roberts *et al.*, "Scaling Up Models and Data with t5x and seqio," *J. Mach. Learn. Res.*, vol. 24, pp. 377:1–377:8, 2023.

[3] E. Choukse, B. Warrier, S. Heath, L. Belmont, A. Zhao, H. A. Khan, B. Harry, M. Kappel, R. J. Hewett, K. Datta *et al.*, "Power stabilization for AI training datacenters," *arXiv preprint arXiv:2508.14318*, 2025.

[4] R. N. Damas, Y. Son, M. Yoon, S.-Y. Kim, and S. Choi, "Subsynchronous Oscillation and Advanced Analysis: A Review," *IEEE Access*, vol. 8, pp. 224 020–224 032, 2020.

[5] E. Guillo-Sansano, M. H. Syed, A. J. Roscoe, G. M. Burt, and F. Coffele, "Characterization of Time Delay in Power Hardware in the Loop Setups," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 3, pp. 2703–2713, 2021.

[6] W. Ren, M. Steurer, and T. L. Baldwin, "Improve the Stability and the Accuracy of Power Hardware-in-the-Loop Simulation by Selecting Appropriate Interface Algorithms," in *2007 IEEE IAS Industrial & Commercial Power Systems Technical Conference*, 2007, pp. 1–7.

[7] D. Rimorov, J. R. Forbes, O. Tremblay, and R. Gagnon, "Robust impedance emulation for transmission line interface in power-hardware-in-the-loop applications: Optimal filter approach," *IEEE Open Journal of the Industrial Electronics Society*, vol. 6, pp. 158–169, 2025.

[8] X. Wu, S. Lentijo, and A. Monti, "A novel interface for power-hardware-in-the-loop simulation," in *2004 IEEE Workshop on Computers in Power Electronics, 2004. Proceedings.*, 2004, pp. 178–182.

[9] R. Mirzahosseini, E. Tara, Y. Zhang, and R. Iravani, "An embedded approach towards power hardware-in-loop (phil) simulation of grid connected inverters (gcis)," in *2024 9th IEEE Workshop on the Electronic Grid (eGRID)*, 2024, pp. 1–6.

[10] J. Sun, S. Wang, J. Wang, and L. M. Tolbert, "Dynamic model and converter-based emulator of a data center power distribution system," *IEEE Transactions on Power Electronics*, vol. 37, no. 7, pp. 8420–8432, 2022.

[11] North American Electric Reliability Corporation, "Reliability guideline: Forced oscillation monitoring & mitigation," North American Electric Reliability Corporation, Atlanta, GA, USA, Tech. Rep., Sep. 2017.