Analytical Design of a Numerical Stabilizer for V-ITM Power Hardware-in-the-Loop Applications

Lucas Braun*, Raphael Isidor Früh, Michael Suriyah, Thomas Leibfried
Institute of Electric Energy Systems and High-Voltage Technology (IEH)
Karlsruhe Institute of Technology (KIT)
Karlsruhe, Germany, *Lucas.Braun@KIT.edu

***Abstract*—Power hardware-in-the-loop (PHIL) simulations enable real-time interaction between numerical models of interest (MOI) and physical hardware under test (HuT), but are prone to numerical oscillations caused by the trapezoidal integration of simulated inductances. These oscillations can lead to voltage overshoots, posing a significant risk to the HuT. This paper introduces a mathematical design methodology for a simulated parallel damping resistor, referred to as a numerical stabilizer, that analytically links the simulation parameters to a desired oscillation attenuation at the voltage-type (V-) ideal transformer model (ITM) interface algorithm (IA) in low-voltage ride through (LVRT) scenarios. This enables the analytical dimensioning of the stabilizer to limit the voltage overshoot to a predefined value without empirical tuning. Experimental validation in a three-phase PHIL setup confirms that the proposed approach effectively reduces the maximum overshoot while maintaining the highest possible PHIL voltage accuracy. Furthermore, a correction factor is introduced to account for real-world deviations, ensuring robust protection of the HuT. The presented method provides an analytical foundation for the systematic stabilization of V-ITM PHIL simulations in LVRT applications.**

***Index Terms*—Power hardware-in-the-loop, real-time simulation, numerical stabilizer**

I. Introduction

Power hardware-in-the-loop (PHIL) provides a test environment in which real components are interfaced with a real-time simulation through power amplifiers (PAs). While actual currents flow and voltages are applied in the hardware under test (HuT), the simulated model of interest (MOI) is computed in real-time using user-defined discrete time steps. The resulting setpoints are then transmitted to the PA, which reproduces the simulated behavior in the physical domain. To ensure a stable and accurate coupling between the MOI and the HuT, an appropriate interface algorithm (IA) must be selected depending on the specific application. However, a fundamental trade-off exists between stability, bandwidth, dynamic, and accuracy. The most widely used and straightforward IA is the ideal transformer model (ITM). Although simple to implement, ITM is prone to stability limitations, as discussed in [1]. Nevertheless, within this work, the ITM is operated exclusively in a stable regime. In addition to the risk of instability in PHIL setups, another undesired phenomenon can occur: numerical oscillations. These arise because the discrete computations of the MOI are performed in digital real-time simulators (DRTS) using the trapezoidal rule, a widely used numerical integration method. The trapezoidal rule is commonly applied as it offers a favorable trade-off between computational effort and numerical accuracy. However, it inherently introduces numerical oscillations that may occur during abrupt state transitions in combination with simulated inductances. This effect can be mitigated by introducing a simulated damping resistor in parallel with the simulated inductance, as demonstrated for purely simulated systems in [2].

In PHIL setups, numerical oscillations are of greater concern since the resulting high oscillatory overvoltage is directly transmitted as a setpoint to the PA. In the absence of an integrated voltage limitation within the PA, this overvoltage is applied directly to the HuT, potentially leading to its destruction. In [3] and [4], it is demonstrated using a real PHIL setup that introducing a damping resistor in the simulation reduces the voltage amplitude of the numerical oscillation. However, this analysis remains qualitative and does not provide a predictive estimation of the expected voltage overshoot at the HuT as a function of the system parameters.

Several studies have addressed stability and accuracy issues in PHIL systems. [1] and [5] investigated the impact of time delay and IA selection on PHIL stability, providing analytical criteria for stable operation of the ITM IA. Other approaches rely on virtual impedance or time delay compensation to improve numerical behavior [6] [7], while filtering and damping impedance methods have also been proposed to avoid instability [8], [9]. However, these methods typically focus on instability rather than on numerical oscillations caused by the trapezoidal integration of inductive components. Furthermore, they often require empirical tuning or controller modification, limiting their analytical predictability.

In contrast, this paper presents the mathematical derivation of an equation to calculate the expected voltage overshoot caused by numerical oscillations across the HuT for the Voltage-Type (V-) ITM IA. Additionally, a practical design formula is proposed that enables the determination of a simulated damping resistor to limit the voltage overshoot to a user-defined value at low-voltage ride through (LVRT) scenarios, which greatly improves practical application. The paper further illustrates how the choice of the discrete sampling rate and the component parameters of the setup influence the amplitude of the numerical oscillations. Using a PHIL setup, the influence of the circuit and simulation parameters on the oscillation overvoltage is investigated in both simulation and experiment. The comparison between simulated results and real measurements

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leads to the determination of a correction factor, which is required for practical design to protect the real HuT from overvoltages caused by inaccuracies and parasitic effects. The theoretical design approach is validated using a three-phase PHIL setup.

II. Trapezoidal Rule

The impedance Z_{L} of an inductor L is defined by the following continuous-time transfer function:

$$\mathrm{Z_L(s)} = \mathrm{V_L(s)/I_L(s)} = s\,L \tag{1}$$

The discretization scheme based on the trapezoidal approximation is defined as follows:

$$s \approx \frac{2}{\Delta t}\frac{z-1}{z+1} \tag{2}$$

The discretization step size Δt corresponds to the simulation sample time T_{DRTS} of the DRTS:

$$\Delta t = T_{\mathrm{DRTS}} \tag{3}$$

By substituting (2) and (3) into (1), the following discrete difference equation for the inductance L_{Sim} simulated in the DRTS is obtained:

$$\frac{2L_{\mathrm{Sim}}}{T_{\mathrm{DRTS}}}(i_n - i_{n-1}) = u_n + u_{n-1} \tag{4}$$

This equation includes not only the present voltage and current values (n), but also those of the previous discrete time step ($n-1$). In the DRTS, the inductor is represented using the companion model, which consists of a series connection of a voltage source and an equivalent resistance $R_{\mathrm{eq,L}}$:

$$R_{\mathrm{eq,L}} = 2L_{\mathrm{Sim}}/T_{\mathrm{DRTS}} \tag{5}$$

For a discrete current change $(i_n - i_{n-1})$ through the simulated inductance L_{Sim}, the equivalent resistance $R_{\mathrm{eq,L}}$ is used to calculate the voltage u_n across the companion model, whose value is additionally influenced by the previous voltage u_{n-1}. When transitioning from one steady-state condition to another, the voltage begins to exhibit numerical oscillations.

A. Experimental Setup

To illustrate this effect, the PHIL measurement setup shown in Fig. 1 is employed, which is based on the V-ITM IA. In this widely adopted interface algorithm, the voltage V_{Sim} is supplied on the simulation side. In this configuration, the simulated grid impedance is modeled in a simplified manner using R_{Sim} and L_{Sim}. Based on the aforementioned parameters and the simulated current I_{RTS}, the voltage V_{RTS} across the simulated ideal controlled current source is calculated and subsequently applied to the linear HuT through a physical PA. The resulting current I_{HuT} is then measured and fed back into the simulation, where it defines the updated value of I_{RTS}. This computation is performed cyclically in real-time with the discretization step size T_{DRTS}.

The laboratory setup employs linear APS10000 power amplifiers from Spitzenberger & Spies in combination with an OPAL-RT OP4510 DRTS. To reduce time delays within the control loop, the PA signals are transmitted optically via the SFP interface using the Aurora protocol. The parameters and values are listed in Table I. The selected voltages and impedances are chosen such that the PA does not enter voltage limitation and the V-ITM control loop remains stable, ensuring the focus is on numerical oscillations and not affected by high-frequency components caused by instability. In the MOI, closing the switch SW generates a HuT LVRT, which induces the numerical oscillations.

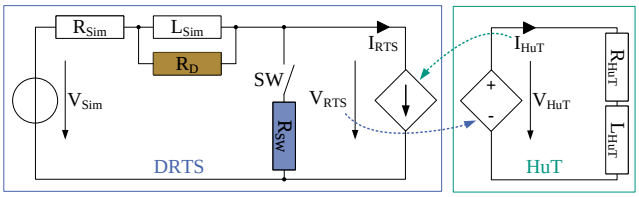

Fig. 1. Equivalent circuit of the V-ITM PHIL setup for generating an LVRT with SW (parameters in Table I)

TABLE I
PHIL Experimental Parameters

$\mathbf{V_{Sim}}$ $\mathrm{V_{(RMS)}}$	$\mathbf{f_{Sim}}$ Hz	$\mathbf{R_{Sim}}$ mΩ	$\mathbf{L_{Sim}}$ μH	$\mathbf{R_{SW}}$ mΩ	$\mathbf{R_{HuT}}$ Ω	$\mathbf{L_{HuT}}$ mH	$\mathbf{T_{DRTS}}$ μs
Single-Phase							
80	0	100	3.5	100	8.2	10.8	10
Three-Phase (phase values)							
100	50	100	1	1	33	2.6	10

B. Practical Problem Description

In Fig. 2, the switch SW is opened at time $t=0$. Without the simulated R_D, numerical oscillations occur, which arise from the trapezoidal rule after a state transition. The voltage oscillates undamped around the computed steady-state value with the following frequency:

$$f_{\mathrm{Osz}} = (2 \cdot \mathrm{T_{DRTS}})^{-1} = (2 \cdot 10\,\mu\mathrm{s})^{-1} = 50\,\mathrm{kHz} \tag{6}$$

The voltage overshoot resulting from the state transition is particularly critical in PHIL applications, as the overvoltage calculated in the simulation is directly transmitted as a setpoint to the PHIL PA and physically applied, which in the worst case can damage the HuT and prevent stable PHIL operation. The measurement results in Fig. 2 illustrate this issue: The peak voltage of the undamped oscillation is 356.5 V, while the steady-state reference value is only 79.3 V (450 %). From (4), it becomes evident that the calculated overvoltage depends on $R_{\mathrm{eq,L}}$ according to (5). The simulated inductance L_{Sim} and the simulation sample time T_{DRTS} directly affect the overvoltage.

Fig. 3 shows that doubling T_{DRTS} results in the same overshoot as halving L_{Sim}. If the inductance in the simulation cannot be reduced, it is therefore advisable to increase the simulation sample time to decrease the oscillation amplitude, although this comes at the expense of time accuracy. In addition to these parameters, the numerical stabilizer is presented next, which can significantly reduce the overvoltage.

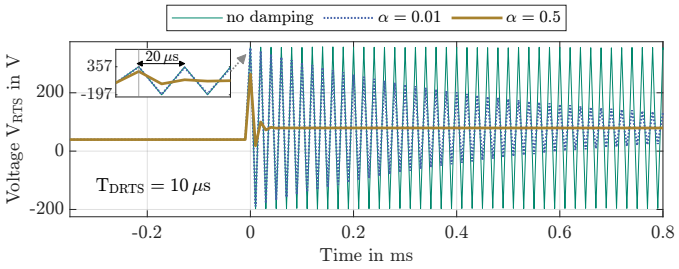

Fig. 2. Experiment: Numerical oscillations with and without R_D (see Table I)

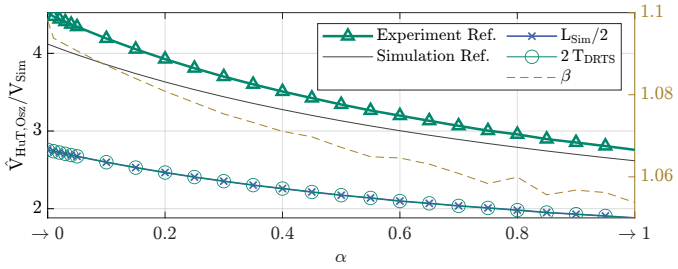

Fig. 3. Experiment: Relative numerical oscillation overvoltage for different α (see Table I) and resulting correction factor β according to (10)

III. Numerical Stabilizer

To damp the numerical oscillations according to [2], a simulated damping resistor R_D is connected in parallel to the simulated inductance L_{Sim}. The continuous-time transfer function is given by:

$$Z_D(s) = V_D(s)/I_D(s) = s\,L_{Sim}R_D/(s\,L_{Sim} + R_D) \quad (7)$$

By substituting (2) and (3) into (7) and applying the following design rule for R_D

$$R_D = 2L_{Sim}/(\alpha T_{DRTS}) \quad (8)$$

the new difference equation is obtained as:

$$\frac{2L_{Sim}}{T_{DRTS}}(i_n - i_{n-1}) = \underbrace{(1+\alpha)}_{\text{Weight (n)}}\,u_n + \underbrace{(1-\alpha)}_{\text{Weight (n}-1\text{)}}\,u_{n-1} \quad (9)$$

The choice of the parameter α is critical and, depending on the desired damping, lies between 0 and 1, where $\alpha = 0$ corresponds to the trapezoidal rule and $\alpha = 1$ corresponds to the backward Euler method. The parameter α thus defines the weighting between the voltage value of the actual and the previous time step. A larger α decreases R_D according to (8) and gives more weight to the actual voltage value, resulting in stronger damping of the oscillations. The calculated equivalent resistance of the parallel connection of R_D and $R_{eq,L}$ decreases accordingly, which reduces the equivalent voltage of the new companion model. For smaller values of α, therefore larger values of R_D, the trapezoidal rule dominates, resulting in lower damping.

Fig. 2 shows the damping behavior of the numerical oscillation with the damping resistor R_D after opening the switch SW of the PHIL setup according to Fig. 1 and Table I at time $t = 0$. For $\alpha = 0.01$, the maximum overshoot relative to the steady-state value is reduced to 353.7 V (450 %→446 %), and for $\alpha = 0.5$ to 264.2 V (450 %→333 %).

Fig. 3 shows that the equivalent resistance of the companion model, and thus the amplitude, also depends on L_{Sim} and T_{DRTS} in the damped case ($0 < \alpha < 1$), in addition to α. Also the measurement results show that doubling T_{DRTS} yields the same results as halving L_{Sim}.

IV. Stabilizer Design for PHIL Applications

Equation (11) is obtained for the numerical oscillation overvoltage $\hat{V}_{HuT,Osz}$, which is computed based on L_{Sim} in combination with the trapezoidal approximation. It should be noted that $\hat{V}_{Sim}$ may also correspond to a negative peak value, resulting in a negative HuT overvoltage. The basis for this is the simplified V-ITM PHIL setup shown in Fig. 1, including the integrated damping resistor R_D. In Fig. 3, the measured normalized voltage $\hat{V}_{HuT,Osz}$ is compared with the voltage calculated according to (11). The measurement results show a deviation of up to +10 % from the calculated values for the used PHIL laboratory setup, which can be attributed to current measurement inaccuracies, hardware impedance tolerances, and measurement noise. Due to this deviation, a correction factor β is introduced to provide a safety margin for practical design, ensuring protection of the HuT against excessive numerical oscillation voltages. The determination of β must be carried out for the individual laboratory setup.

$$\beta = \hat{V}_{HuT,Osz,Meas.}/\hat{V}_{HuT,Osz,Calc.} = 1.1 \quad (10)$$

A. Phase Influence

Fig. 4 shows the absolute value $\hat{V}_{HuT,Osz}$ of the numerical oscillation overvoltage as a function of the phase angle of V_{Sim} at which the LVRT recovery occurs. The relationship between the instantaneous value of V_{Sim} and $\hat{V}_{HuT,Osz}$ is evident: the higher the absolute value of V_{Sim}, the higher $\hat{V}_{HuT,Osz}$. There are deviations between the measured values and those calculated according to (11). The deviation at the absolute maximum of V_{Sim} is critical, as it represents the highest absolute HuT voltage and thus the greatest potential risk. This deviation is $\beta = 1.09$ and must be taken into account in the practical design of α.

B. Parameter Influence

The effect of the additional PHIL parameters shown in Fig. 1 on the amplitude of the numerical oscillation voltage, as defined in (11), is illustrated in the following. Fig. 5 shows that an increase in the simulated inductance L_{Sim} leads to a significant increase in $\hat{V}_{HuT,Osz}$. A smaller α increases this effect. Selecting a small L_{Sim} in the PHIL setup is advisable, provided that the desired accuracy can still be maintained. Fig. 6 shows that increasing the simulation sample time T_{DRTS} leads to a reduction in $\hat{V}_{HuT,Osz}$. However, the accuracy is reduced in this case. The described relationship that doubling T_{DRTS} and halving L_{Sim} have the same effect on $\hat{V}_{HuT,Osz}$ becomes apparent here. Fig. 7 illustrates how $\hat{V}_{HuT,Osz}$ is

$$\hat{V}_{\mathrm{HuT,Osz}} = \hat{V}_{\mathrm{Sim}} \frac{R_{\mathrm{HuT}} \left((R_{\mathrm{Sim}} R_{\mathrm{SW}} + R_{\mathrm{Sim}} R_{\mathrm{HuT}} + R_{\mathrm{SW}} R_{\mathrm{HuT}}) + \frac{2L_{\mathrm{Sim}}}{T_{\mathrm{DRTS}}(\alpha+1)} (R_{\mathrm{SW}} + R_{\mathrm{HuT}}) \right)}{\left(R_{\mathrm{Sim}} + R_{\mathrm{HuT}} + \frac{2L_{\mathrm{Sim}}}{T_{\mathrm{DRTS}}(\alpha+1)} \right) \left(R_{\mathrm{Sim}} R_{\mathrm{SW}} + R_{\mathrm{Sim}} R_{\mathrm{HuT}} + R_{\mathrm{SW}} R_{\mathrm{HuT}} \right)} (\cdot \beta) \tag{11}$$

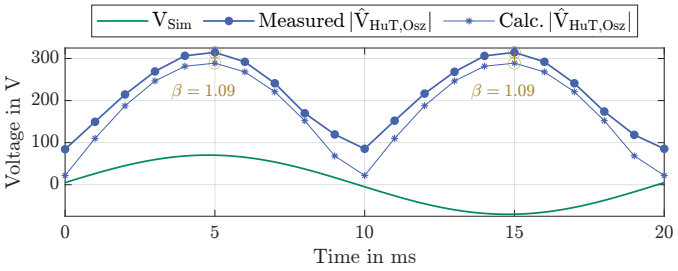

Fig. 4. Experiment: Influence of the phase angle on the maximum overvoltage of the numerical oscillation (see Table I)

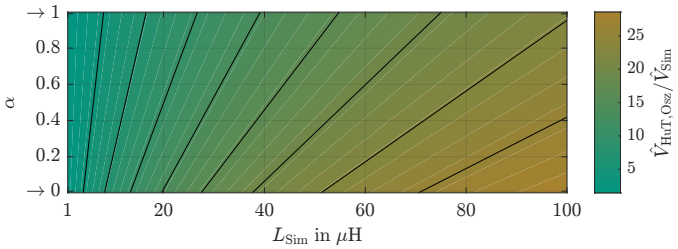

Fig. 5. Simulation: Maximum overvoltage of the numerical oscillations according to (11) for different α and L_{Sim} (see Table I)

affected by the choice of the free parameters α and T_{DRTS} for given simulation values. The maximum overvoltage of the numerical oscillation can thus be adjusted accordingly.

V. Validation

For the validation of the mathematical relationship for $\hat{V}_{\mathrm{HuT,Osz}}$ presented in (11), the PHIL setup shown in Fig. 1 is used and extended to a three-phase AC system. The simulation parameters are listed in Table I and the three input voltages V_{Sim} are symmetrical with a phase shift of 120°. The neutral point of the HuT is grounded. A LVRT is applied to phase A by closing the low-impedance switch SW at time $t = 15\,\mathrm{ms}$. At $t = 75\,\mathrm{ms}$, the switch is opened again.

Fig. 8 shows the three HuT voltages without the simulated damping resistor R_{D}. Due to the state transition caused by

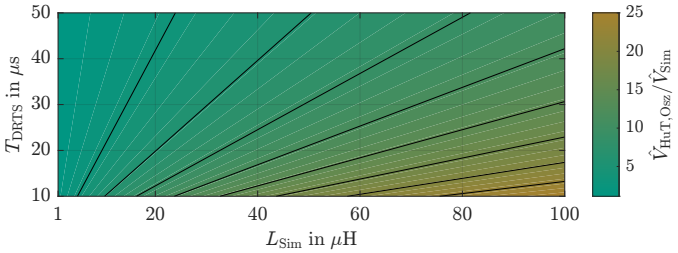

Fig. 6. Simulation: Maximum overvoltage of the numerical oscillations according to (11) for different T_{DRTS} and L_{Sim} at $\alpha = 0.5$ (see Table I)

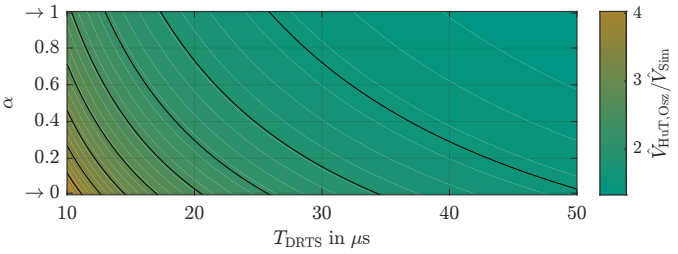

Fig. 7. Simulation: Maximum overvoltage of the numerical oscillations according to (11) for different T_{DRTS} and α (see Table I)

opening the switch, the voltage of the affected phase exhibits numerical oscillations. The measured maximum value $\hat{V}_{\mathrm{HuT,Osz,Meas.}}$ is 418.4 V (296 %). The maximum voltage calculated according to (11) is 417.7 V, which results in a relative deviation of 0.17 %. For the unaffected phases, no numerical oscillations occur due to the grounded neutral point.

For further validation, the voltage across the HuT $\hat{V}_{\mathrm{HuT,Osz}}$ is limited to a maximum of 400 V. Therefore, with $\beta = 1$, α=0.07 is calculated according to (11). The corresponding damping resistor $R_{\mathrm{D}} = 2.86\,\Omega$ is calculated according to (8) and integrated into the simulation. Fig. 9 shows the measurement results of the PHIL setup. The measured maximum voltage at the LVRT recovery is $\hat{V}_{\mathrm{HuT,Osz,Meas.}} = 395.8\,\mathrm{V}$, deviating by 1.05 % from the calculated value.

For the final validation step, the previously introduced correction factor β is set to +10 % ($\beta = 1.1$). The maximum allowable HuT voltage is limited to 400 V, thus $\hat{V}_{\mathrm{HuT,Osz}} = 400\,\mathrm{V}$. According to (11), this results in $\alpha = 0.244$, which corresponds to a damping resistor of $R_{\mathrm{D}} = 0.82\,\Omega$ as calculated by (8). The measured HuT voltages in Fig. 10 show a maximum value of $\hat{V}_{\mathrm{HuT,Osz,Meas.}} = 360\,\mathrm{V}$, representing a relative deviation of 10 %, which matches the correction factor β. In this case, the correction factor provides a relevant safety margin with respect to the maximum permissible voltage. In practical PHIL operation, this margin is essential to protect the HuT from overvoltages, as measurement inaccuracies, limited

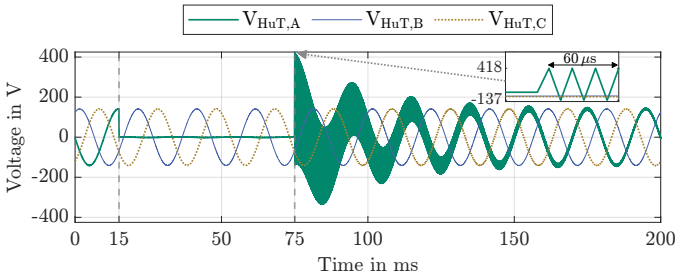

Fig. 8. Experiment: Single-phase LVRT without damping resistor R_{D}. ($\hat{V}_{\mathrm{HuT,Osz,Calc.}} = 417.7\,\mathrm{V}$, $\hat{V}_{\mathrm{HuT,Osz,Meas.}} = 418.4\,\mathrm{V}$) - (see Table I)

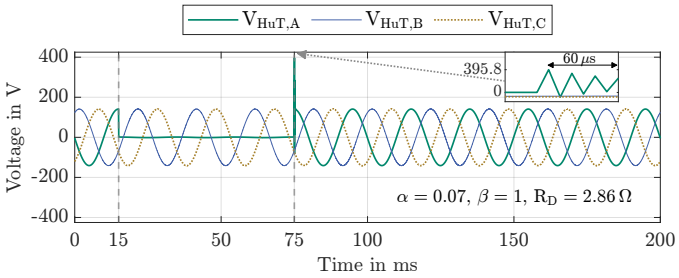

Fig. 9. Experiment: Single-phase LVRT with damping resistor R_D. ($\hat{V}_{HuT,Osz,Calc.} = 400\,V$, $\hat{V}_{HuT,Osz,Meas.} = 395.8\,V$) - (see Table I)

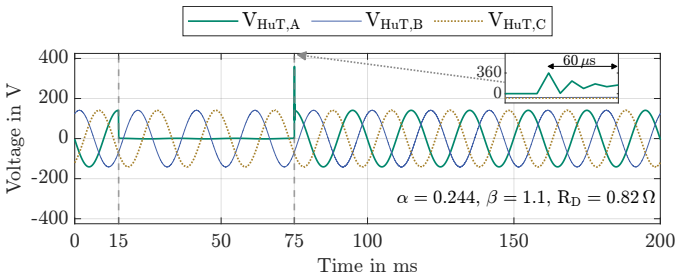

Fig. 10. Experiment: Single-phase LVRT with damping resistor R_D. ($\hat{V}_{HuT,Osz,Calc.} = 400\,V$, $\hat{V}_{HuT,Osz,Meas.} = 360\,V$) - (see Table I)

resolution, and parasitic effects are present in the setup. Hence, β serves as a safety factor for reliable PHIL system design.

A. Generalization

The relationship in (11) can, in theory, be extended to the Current-Type (C-) ITM IA, since it shares the same ideal electrical equivalent circuit. In this IA, the simulated current is provided as a reference signal to the PA, while the measured HuT voltage is fed back into the simulation through an controlled voltage source. However, there are practical reasons that limit its applicability. First, the C-ITM quickly reaches its stability limit during a software-based LVRT, making PHIL operation impossible. The ratio between the HuT impedance and the simulation impedance becomes too large due to the low-impedance simulated switch, causing the system to become unstable, with the stability condition of the C-ITM being reciprocal to the V-ITM condition. Second, for inductive loads, the actual voltage overshoot at the HuT can become high, since the current slew rate in the C-ITM IA can increase significantly. Therefore, for LVRT applications, the C-ITM is only suitable when the voltage dip at the HuT is not generated in the simulation.

Other IAs, such as the advanced V-ITM, partial circuit duplication, or transmission line model, include additional circuit elements such as series or parallel impedances, resulting in a more complex calculation of the HuT voltage affected by numerical oscillations. Consequently, (11) is no longer sufficient for determining the maximum voltage in these cases. The approach assumes linear HuT characteristics and neglects active behavior. These effects will be addressed in future work. Simplifying complex simulated networks into the equivalent circuits in Fig. 1 is only valid within certain limits: In a radial network with a common supply node, the inductances between the supply node and the LVRT node primarily have a negative effect on the oscillation voltage amplitude, as the dominant state change occurs here. Additional series or parallel inductances along this branch can increase the oscillation amplitude. Therefore, they must be damped and, for the calculation according to (11), combined and taken into account.

VI. Conclusion and Outlook

This paper presented an analytical framework for predicting and damping numerical oscillations in PHIL applications using the trapezoidal rule. Although such oscillations are a known artifact of discrete-time integration, their quantitative impact on HuT voltage and overvoltage risk had not been analytically defined for the V-ITM IA in LVRT applications before. The proposed formula establishes an analytical link between PHIL parameters, the damping coefficient, and the resulting HuT overvoltage. By deriving a design equation for a simulated damping resistor, the approach enables control of oscillation amplitude without empirical tuning. Experimental validation in a three-phase PHIL setup confirmed the analytical prediction and showed that the method effectively limits HuT overvoltage while preserving accuracy. A correction factor further ensures robust operation under real-world uncertainties. The methodology provides a analytical basis for designing numerically stable PHIL experiments. Future work will extend this approach to other IAs and HuT to generalize its applicability.

References

[1] W. Ren, M. Steurer and T. L. Baldwin, "Improve the Stability and the Accuracy of Power Hardware-in-the-Loop Simulation by Selecting Appropriate Interface Algorithms," 2007 IEEE/IAS Industrial & Commercial Power Systems Technical Conference, Edmonton, AB, Canada, 2007, pp. 1-7.

[2] W. Gao, E. Solodovnik, R. Dougal, G. Cokkinides and A. P. S. Meliopoulos, "Elimination of numerical oscillations in power system dynamic simulation," Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2003. APEC '03., Miami Beach, FL, USA, 2003, pp. 790-794 vol.2.

[3] S. Hubschneider, "Power-Hardware-in-the-Loop-Systeme als Evaluationsumgebung für Betriebsmittel und Netze der Niederspannung," Dissertation, Karlsruhe Institute of Technology (KIT), IEH, Karlsruhe, Germany, 2023.

[4] L. Braun, S. Kist, D. Eser, M. Suriyah and T. Leibfried, "Stability Improvement of a Dynamic Low-Voltage Power Hardware-in-the-Loop Environment," NEIS 2024; Conference on Sustainable Energy Supply and Energy Storage Systems, Hamburg, Germany, 2024, pp. 27-32.

[5] O. Tremblay, H. Blanchette, R. Gagnon, and Y. Brissette, "Contribution to stability analysis of power hardware-in-the-loop simulators," IET Generation, Transmission & Distribution, vol. 11, no. 9, Jun. 2017.

[6] X. Zha, C. Yin, J. Sun, M. Huang, and Q. Li, "Improving the stability and accuracy of power hardware-in-the-loop simulation using virtual impedance method," Energies, vol. 9, no. 11, Art. no. 974, 2016.

[7] L. Braun, J. Mader, M. Suriyah, and T. Leibfried, "Improvement of positive and negative feedback power hardware-in-the-loop interfaces using Smith predictor," Energies, vol. 18, no. 14, Art. no. 3773, 2025.

[8] S. Resch, J. Friedrich, T. Wagner, G. Mehlmann, and M. Luther, "Stability analysis of power hardware-in-the-loop simulations for grid applications," Electronics, vol. 11, no. 1, Art. no. 7, 2022.

[9] J.-W. Lim, K.-W. Heo, C.-o. Jeon, H. Kim, and J.-H. Jung, "Development of Power Hardware-in-the-Loop Simulation Test-bed to Verify LVDC Grid Stability Using Offline Damping Impedance Design," J. Electr. Eng. Technol., vol. 19, pp. 3297–3308, 2024.