AC Network Fault Characterisation in MMC based HVDC Systems

Pratik Rao
Department of Electrical Engineering
Indian Institute of Technology Bombay
Mumbai, India

Himanshu J. Bahirat
Department of Electrical Engineering
Indian Institute of Technology Bombay
Mumbai, India

***Abstract*— MMC-HVDC has gained popularity in recent years and the ac grid is being redefined with MMC-HVDC interconnections embedded in the larger ac grid. This requires an evolving grid code framework. In recent grid code versions, the fault ride through (FRT) capability has emerged as a critical requirement for converter-based resources, including HVDC, thereby demanding the implementation of suitable control strategies to ensure compliance. These power electronic based systems exhibit different fault characteristics when compared to conventional ac power systems and hence it becomes crucial to study the fault characteristics. In this paper, rectifier side AC faults are characterized based on the FRT operation in PSCAD/EMTDC. These fault characteristics then set the ground for the coordinated protection system design.**

***Index Terms*—AC faults, Fault ride through, MMC-HVDC, Positive sequence injection.**

I. INTRODUCTION

In recent years Modular Multilevel Converter (MMC) has become a favorite choice for High Voltage Direct Current (HVDC) systems, be it interconnection to offshore wind, solar PV or grid interconnections for its obvious advantages [1]-[2]. Eventually, these HVDC systems are expected to interconnect to form multi-terminal DC grids [1], introducing new challenges in the design and operation of AC/DC power systems, particularly concerning existing protection schemes.

Recently, several grid codes (eg. European Network of Transmission System Operators for Electricity (ENTSO-E) [3]) have set out detailed requirements for HVDC interconnection with grid or offshore wind; which requires the HVDC to stay connected to the system in case of faults and provide reactive support to aid the recovery of point of common coupling (PCC) voltage. These require advance control system design for asymmetrical current injection and coordinated FRT strategies. Hence, it is important to analyze the characteristics of AC faults for MMC HVDC systems including these grid code requirements. Research has been conducted focusing on characterization of ac faults at the inverter side [4]-[6] and have recommended FRT strategies, including the use of DC chopper and DC voltage margin control [7]-[9]. In [5], applicability of distance protection as a backup for line faults at the inverter end has been studied. Even though, [5] recognizes that the unique fault characteristics of MMC-HVDC affects the distance protection, it recommends to retain the distance protection for zone II and III. Further, the analysis is based on zero reactive current reference and positive sequence (PS) reactive current injection profile is not considered. In [10], efforts have been made to study the inverter end L-G fault with auto reclose and coordinated approach to ride through the fault has been presented.

However, characterization of rectifier side ac faults has not been extensively explored and it becomes necessary to study these faults as their characteristics tend to differ from the inverter side faults. The rectifier side faults lead to a severe dip in the PCC voltage and rapid reduction in the dc current due to interruption of power from AC side. Efforts are being made to study the rectifier end grid faults based on the mathematical model which is presented in [11]. However, the analysis in [11] is limited to symmetrical faults and it does not consider the grid code requirement to stay connected to the system. Instead, it continues to analyze the fault signatures considering that the overcurrent protection will block the MMC within five milliseconds.

The novelty of this paper lies in analyzing rectifier side ac faults (symmetrical & asymmetrical) in grid connected MMC-HVDC system shown in the Fig. 1 and assessing the impact it may have on conventional ac protection. In HVDC systems, the control and protection are closely integrated, and control strategies significantly influence the fault signatures. This study presents fault signatures for a control system compliant with EU grid code requirements, specifically, the positive sequence injection (PSI) and negative sequence suppression (NSS), highlighting how different LVRT mandates complicate fault characterization and pose challenges in HVDC protection.

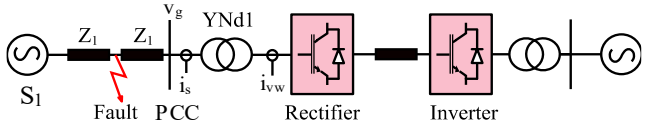


Fig. 1 Representation of simulated MMC-HVDC system

979-8-3315-8138-1

II. LVRT Requirements of the Grid

Several grid codes (including ENTSO-E [3], VDE-AR-N 4120 [12] in Germany, CEA in India) have different interconnection requirements during fault conditions [3], [13], [12]. It is crucial to ensure that a suitable control system which meets the low voltage ride through (LVRT) requirements have been incorporated both under balanced and unbalanced fault conditions to design an efficient protection system. In [14], author has compared different national grid codes and identified considerable differences in the requirements when compared with the EU 2016/1447 [3], [15]. It is also suggested that these grid codes align with the ENTSO-E so that there is homogeneity in the control and protection system. The LVRT requirements and the fault current injection requirements based on EU 2016/1447[15] is adapted in this paper. The ac voltage profile at the PCC during the fault is presented in the Fig. 2. During this fault condition the reactive current is given high priority and the reactive current injection profile illustrated in Fig. 3 is implemented in this paper [14], [13].

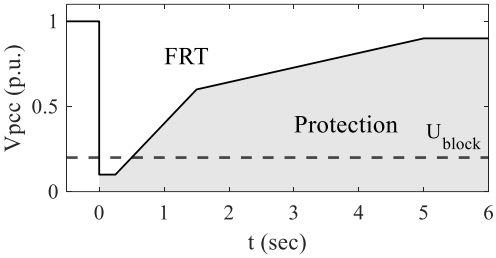


Fig. 2 AC voltage profile during FRT

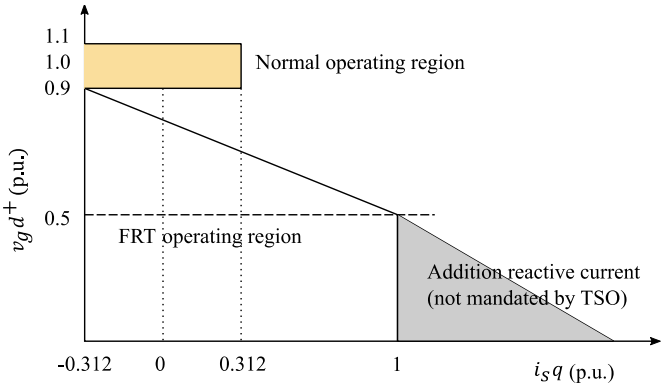


Fig. 3 Positive sequence reactive current injection profile

III. MMC-HVDC Control Strategy

This paper presents a grid connected MMC-HVDC system as shown in Fig. 1. For ease of analysis, it is assumed that the power flows from the rectifier to inverter. A conventional vector current control has limitations during unbalanced operation, as the PCC voltage (v_g) has positive and negative sequence components, the conventional transvector PLL cannot accurately track the angle. To overcome this issue, decoupled double synchronous reference frame (DDSRF) based PLL [16] which uses the positive sequence voltage to track the angle is implemented. Furthermore, the conventional vector current control is inadequate to comply with the LVRT requirement detailed in section-II. Hence, to comply with the LVRT, positive-negative sequence current controller (PNSCC) is implemented as shown in the Fig. 4 which can independently control the respective sequence reactive currents [9], [16].

The rectifier adopts the active power demand to derive the d-axis positive sequence (PS) current reference ($i_s^* d^+$) and ac voltage control (ACVC) to derive the q-axis PS current reference ($i_s^* q^+$) during normal operation. The inverter implements dc voltage control to derive the d-axis current reference for PS ($i_s^* d^+$) and ACVC to derive the q-axis current reference for PS ($i_s^* q^+$) during normal operation. The value of $i_s^* q^+$ is limited between -0.312 to 0.312 p.u. during normal operation (as shown in Fig. 3). The negative sequence (NS) active current ($i_s^* d^-$) references and negative sequence reactive current ($i_s^* q^-$) references are set to zero on both rectifier and inverter end to suppress negative sequence.

During ac grid contingency, the DDSRF will extract the positive and negative sequence component from the PCC voltage and define the current reference based on the LVRT requirement defined in the Grid codes. In this paper, the LVRT characteristic of an HVDC converter station defined in [15] has been implemented. To meet the LVRT, PSI proportional to the voltage drop defined in [16] is implemented as shown in Fig. 4. Hence, in this paper asymmetrical FRT with PSI and NSS is implemented.

The reactive current is calculated from the equation (1),

$$i_s^* q^+ = k * (0.9 - v_g d^+) \tag{1}$$

The relation of d-q axis currents is given as,

$$i_s = \sqrt{(i_s d)^2 + (i_s q)^2} \leq i_{\text{rated}}\ (1\ \text{p.u.}) \tag{2}$$

where,

$$i_s d = i_s d^+ + i_s d^-;\ i_s q = i_s q^+ - i_s q^- \tag{3}$$

The voltage on each submodule (SM) capacitor depends on the charge/ discharge cycle of that SM. Since, no two SMs can have the exact same cycle, the voltages on each SMs are different. These differences in the voltages may result into circulating currents in the MMC. Hence, in addition to the above control, a circulating current controller aimed to reduce the circulating current to zero in normal operation is implemented along with capacitor voltage balancing controller (CVBC) [16]. The block diagram of these controllers is presented in Fig. 4.

IV. Test Scenarios

In this section, the tests scenarios are described and simulated using PSCAD/EMTDC and the fault characteristics during the FRT are discussed. The test system parameters are detailed in Table 1. The DC cable is represented as frequency dependent distributed parameter model to capture high frequency transients. The AC network is modeled as a Thevenin source (S_1) and the ac transmission line is modelled as a lumped R-L representing a weak grid with SCR < 2 at the PCC. The different types of ac faults exhibit different fault characteristics and voltage dips. This paper studies five different rectifier end

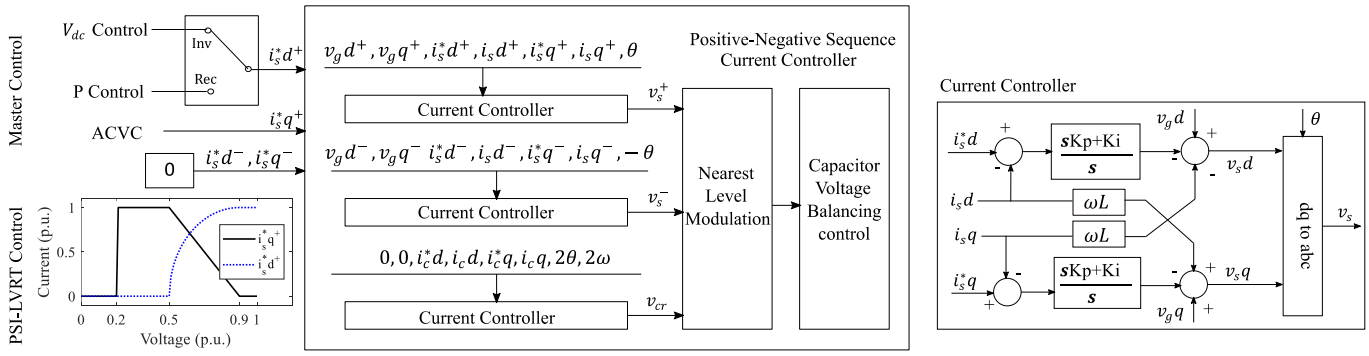


Fig. 4 Implemented HVDC control system architecture

fault scenarios; the scenarios 1 and 2 present the symmetrical faults with low and high fault impedances respectively; scenarios 3–6 present asymmetrical faults. The fault is applied at the mid-point of the ac transmission line as shown in the Fig. 1 at t=0.05s. The d-q axis currents are per unitized on a base of 600MVA. Scenarios 1-5 are simulated based on the PSI-LVRT characteristics shown in Fig. 4 and scenario 6 is presented with positive negative sequence injection (PNSI) to highlight the impact of different LVRT mandates on fault signatures.

TABLE 1 MMC HVDC parameters used for fault studies

Parameters	**Values**
Configuration	Symmetric Monopole
Power Rating	500 MW/600MVA
DC Voltage Rating	500 kV
DC Cable length	500 km
Transformer	YNd11 (230kV/280kV)
Transformer Leakage Impedance	0.12 p.u.
Number of SMs/ arm	5
Arm Inductance	0.0416 H
Arm Resistance	0.32667 H
SM Capacitance	960 µF
SCR of S_1	< 2 (Weak Grid)
X/R of S_1	approx. 20

A. *Symmetrical Faults*

In this section, symmetrical ac faults have been modelled and the system response for a solid three phase to ground fault and a high impedance fault (50 Ω) has been studied.

1) *Scenario1: Solid three phase to ground (LLL-G) fault*

As shown in the Fig. 5(a), when a solid three phase to ground fault is applied, the ac voltage (v_gd^+) dips below the blocking level (U_{block} = 0.2pu). Hence, based on the LVRT control the PS d-q current references ($i_s^*d^+$ and $i_s^*q^+$) are set to zero. The negative sequence variables are zero as it is a balanced fault. However, based on different protection strategies the MMC can be blocked immediately when the voltage is less than U_{block} or it can stay connected until the undervoltage relay (coordinated with LVRT) operates.

2) *Scenario 2: High impedance three phase to ground fault*

Fig. 5(b) shows that during a high impedance three phase to ground fault (of 50Ω), the ac voltage (v_gd^+) dips to 0.63 p.u. and hence, the $i_s^*d^+$ and $i_s^*q^+$ are calculated according to the PSI-LVRT current characteristics indicated in Fig. 4, increasing $i_s^*q^+$ from 0.25 p.u. to 0.675 p.u. and decreasing $i_s^*d^+$ according to the eq. (2). Here, the scheme continues operation with reduced power. The negative sequence variables are zero as it is a balanced fault.

B. *Unsymmetrical Faults*

In this section, unsymmetrical faults in the ac network are studied and the system response during the fault is presented.

1) *Scenario 3: Line to Line to Ground (LL-G) fault*

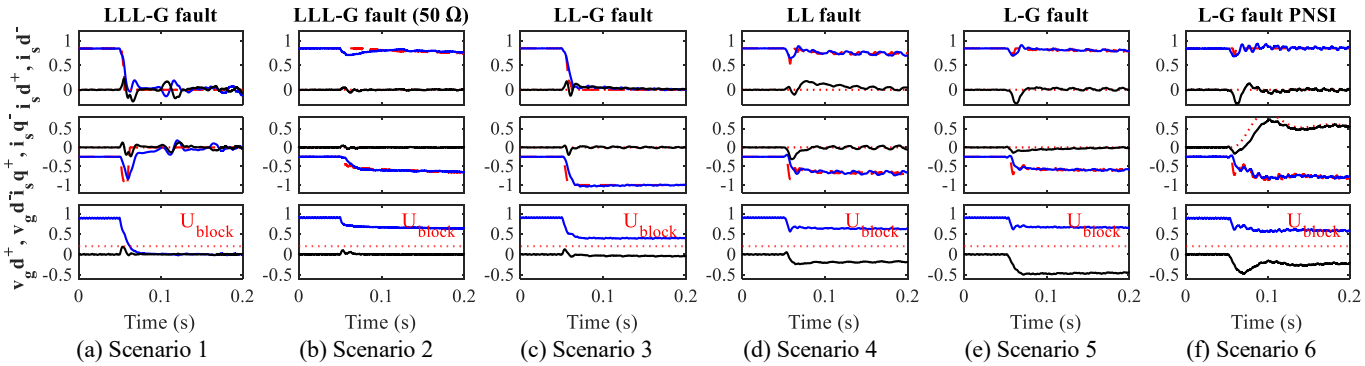
Fig. 5(c) shows that during LL-G fault, the ac system voltage (v_gd^+) drops to 0.38 p.u. Hence, the LVRT control reduces the active current reference ($i_s^*d^+$) to zero simultaneously increasing the reactive current reference ($i_s^*q^+$) to 1 p.u based on PSI-LVRT. Since, this is an unbalanced fault the negative sequence voltage (v_gd^+) increases to 0.085 p.u., however the negative sequence suppression control maintains the negative sequence currents (i_sq^- and i_sq^+) at zero.

2) *Scenario 4: Line to Line (LL) fault*

Fig. 5(d) shows that during LL fault, the ac system voltage (v_gd^+) dips to 0.56 p.u. and the negative sequence voltage increases to 0.24 p.u. Based on the PSI-LVRT characteristics, $i_s^*q^+$ increases proportional to the voltage and $i_s^*q^-$ is set to zero. Further, unbalance in the SM voltages of the three phases, which can be inferred from the average upper arm voltages (V_{TA}, V_{TB}, V_{TC}) shown in the Fig. 7(a), leads to increase in the circulating currents. However, it can be observed from Fig. 7(a) that the circulating current controller and CVBC eventually balance these arm voltages suppressing the circulating current by certain amount within a second. Despite the efforts the combined interaction of negative sequence voltage and circulating current is observed on d-q axis currents as seen in the Fig. 5(d) and on the DC voltage (V_{dc}), as seen in Fig. 7(a), where a 100Hz oscillation increases V_{dc} to 1.1 p.u.

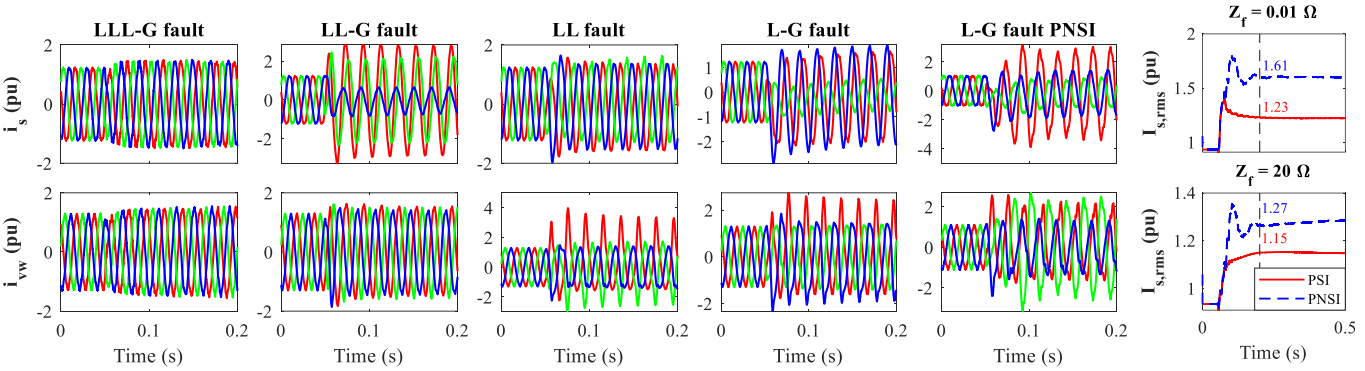
3) *Scenario 5: Line to ground (L-G) fault*

Fig. 5(e) shows that when a line to ground fault is simulated, it is observed that the ac voltage (v_gd^+) dips to 0.61 p.u. hence the corresponding d-q axis current references change to meet the LVRT. However, the negative sequence voltage (v_gd^-) increases to 0.495 which is highest among unbalance faults, the negative sequence introduces 100Hz oscillation. Further, the effect of unbalance in the SM voltages on the DC voltage and the arm voltages are shown in the Fig. 7(b).



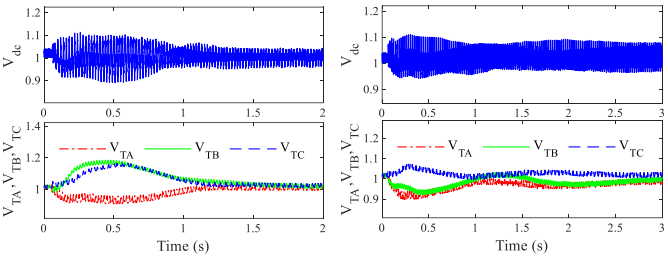
(a) Scenario 1 (b) Scenario 2 (c) Scenario 3 (d) Scenario 4 (e) Scenario 5 (f) Scenario 6

Fig. 5 Fault characteristics for the fault scenarios 1–6 (blue: positive sequence; black: negative sequence).



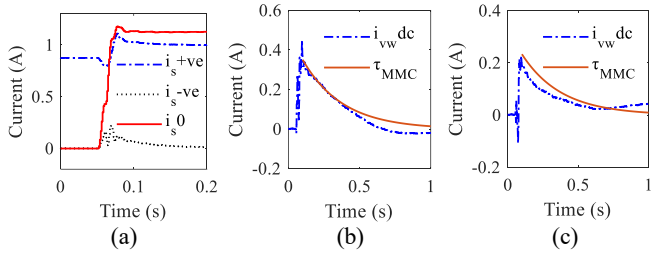
(a) Scenario 2 (b) Scenario 3 (c) Scenario 4 (d) Scenario 5 (e) Scenario 6 (f)

Fig. 6 (a)-(e) Three-phase currents for fault scenarios 2–6 (red: phase a; green: phase b; blue: phase c); (f) Rms current for fault scenario 5–6.



(a) Scenario 4 (b) Scenario 5

Fig. 7 Effect of unbalance faults on DC and average arm voltage.



(a) (b) (c)

Fig. 8 Current plots (a) Sequence components of i_s during LL-G fault; (b) dc component in i_{vw} during LL fault; (c) dc component in i_{vw} during L-G fault (scenario 5)

4) *Scenario 6: L-G fault with PNSI*

Fig. 5(f) shows the simulation results for a L-G fault when positive negative sequence injection (PNSI) based LVRT strategy is implemented. This scenario is presented to highlight the impact of the PSI and PNSI strategies on the fault signatures. It is observed that with this strategy the negative sequence voltage ($v_g d^-$) reduces to 0.23 compared to 0.495 in scenario 5.

C. *Characterization of fault signatures and challenges to conventional protection schemes*

Fig. 6(a)-(e) illustrates the three phase ac fault currents at the PCC (i_s) and at the transformer secondary currents (i_{vw}) for different faults simulated in this section. It is observed from Fig. 6(a), that during the balanced LLL-G high impedance fault, both i_s and i_{vw} are balanced; the current magnitude increases due to reactive current ($i_s q^+$) injection. However, the currents do not exceed 1 p.u. (i.e., peak value of 1.414).

During the LL-G fault it is observed from Fig. 6(b), that the i_{vw} is balanced but, i_s exhibits unbalance due to the presence of zero sequence current as shown in the Fig. 8(a). As a result of the zero-sequence current, i_s currents in the faulted phases (i.e., a and b phases) exceed 2 p.u. and the current in the healthy phase is reduced. To continue LVRT during this fault, coordination with transformer earth-fault protection is necessary as the increased zero-sequence current shown in Fig. 8(a) may lead to operation of earth-fault relay.

During LL fault, dc offset is observed in the i_{vw} and faulty phase peak current increases to 4 p.u. as seen in Fig. 6(c). From Fig. 8(b), it is observed that the dc component is governed by, the time constant, τ_{MMC}, which is the combination of the transformer leakage impedance and the L/R ratio of the MMC arm. As a result of the energy asymmetry in the three phases, it is observed from Fig. 7(a), that the SM voltages become

unbalanced during the fault, leading to increase in the circulating currents (2ω component). If these circulating currents and SM voltage unbalance are not addressed, it may sustain the dc offset in i_{vw}. However, with effective capacitor voltage balancing control and circulating current control, it is interpreted from the average upper arm voltages shown in Fig. 7(a) that the SM voltages are balanced in about a second. However, it is crucial to coordinate this characteristic with conventional overcurrent relay & transformer protection schemes to avoid block and trip due to unnecessary protection and continue LVRT. The transformer differential relay will see differential bias and hence it is important to appropriately implement the restraint current in the differential relay to avoid false tripping during FRT of asymmetrical faults.

Fig. 6(d) and Fig. 6(e) represent the fault signatures during a L-G fault with PSI and PNSI respectively. From Fig. 6(d) it is observed that the i_{vw} currents have dc offset in the beginning for the same reasons stated in the above paragraph for LL fault. From Fig. 8(c), it is observed that the dc component is governed by the combined L/R ratio of the MMC & the transformer (τ_{MMC}). Even after deploying capacitor voltage balancing control and circulating current control, the dc offset cannot be completely eliminated, but is suppressed to about 0.03 p.u. This dc offset may reflect in transformer differential relay and hence has to be accounted for, as discussed above for LL fault.

Fig. 6(d), shows that the i_s currents are unbalanced due to presence of zero-sequence components; but under PSI, the faulty phase cannot be identified by looking at the instantaneous i_s currents. In contrast, for a L-G fault under PNSI, Fig. 6(e) shows that the i_s currents, clearly distinguish the faulty phase (phase a). This observation under PSI, may have implications on the single-phase auto-reclose logic.

Fig. 6(f) compares the rms currents during a L-G fault under PSI and PNSI. From Fig. 6(f) it can be seen that during PSI, the rms fault currents have lower magnitude (1.23 p.u. for a solid L-G fault and 1.15 p.u. for a high impedance fault) which may lead to reduced sensitivity in conventional transmission protections like overcurrent and distance protection schemes. Due to low value of current the apparent impedance increases which may lead to under reach during high impedance L-G faults. In PNSI, the current magnitude is higher ((1.61 p.u. for a solid L-G fault and 1.27 p.u. for a high impedance fault) providing better protection visibility and fault discrimination.

V. CONCLUSION

This paper evaluates the rectifier side ac fault in MMC-HVDC system connected to the grid, taking into account the PSI-LVRT requirements. Symmetrical and unsymmetrical fault characteristics are reviewed and following can be concluded – While PSI ensures grid compliance, it significantly degrades the dependability of conventional protection due to symmetrical nature and lower fault currents. The dc offset in the ac fault currents during asymmetrical faults has to be accounted for in conventional transformer differential protection. It is observed that, during unbalance faults, ac transformer currents and dc voltages show peculiar behaviors which may interfere with other protection. Hence, to achieve effective FRT, the coordination of ac and dc protection systems should be investigated. These challenges provide opportunities for advanced protection strategies, including adaptive distance relays, undervoltage relay coordinated with the LVRT characteristics and sequence injection based pickup levels for overcurrent protection.

REFERENCES

[1] D. Van Hertem, O. Gomis-Bellmunt, and Liang Jun, *HVDC Grids: For Offshore and Supergrid of the Future*. Hoboken, New Jersey: John Wiley & Sons, Inc., 2016. [Online]. Available: www.wiley.com.

[2] C. Barker and R. Gupta, "Completing the Circuit: Integration of Offshore Wind Farms into the Grid using High Voltage dc Technology," *IEEE Power and Energy Magazine*, vol. 22, no. 5, pp. 31–37, 2024.

[3] "ENTSO-E Network Code for Requirements for Grid Connection Applicable to all Generators This document reflects the work done by ENTSO-E in line with the ACER Framework Guidelines on Electricity Grid Connections," 2013. [Online]. Available: www.entsoe.eu

[4] E. Bian, H. Xu, C. Kang, J. Liu, Z. Wang, and S. Fan, "Research on the fault characteristics of HVDC with wind farm," in *2017 IEEE Conference on Energy Internet and Energy System Integration (EI2)*, Beijing, China, 2017, pp. 1–5.

[5] K. Xu, Z. Zhang, Q. Lai, J. Han, X. Yin, and W. Liu, "Study on fault characteristics and distance protection applicability of VSC-HVDC connected offshore wind power plants," *International Journal of Electrical Power and Energy Systems*, vol. 133, Dec. 2021.

[6] H. Zhou, W. Yao, K. Sun, X. Ai, J. Wen, and S. Cheng, "Characteristic Investigation and Overvoltage Suppression of MMC-HVDC Integrated Offshore Wind Farms under Onshore Valve-Side SPG Fault," *IEEE Transactions on Power Systems*, vol. 39, no. 1, pp. 1346–1359, Jan. 2024

[7] J. Li, B. Yang, B. Xie, and Y. Zhang, "AC Fault Ride-through Control Strategy and Fault Characteristics Analysis of AC / DC System Based on MMC-MTDC," in *2023 3rd New Energy and Energy Storage System Control Summit Forum, NEESSC 2023*, Institute of Electrical and Electronics Engineers Inc., 2023, pp. 487–491.

[8] S. Cao *et al.*, "Energy dissipation of MMC-HVDC based onshore wind power integration system with FB-DBS and DCCB," *IET Renewable Power Generation*, vol. 14, no. 2, pp. 222–230, Feb. 2020.

[9] S. D. Tavakoli, E. Prieto-Araujo, and O. Gomis-Bellmunt, "AC Fault Ride Through in MMC-Based HVDC Systems," *IEEE Transactions on Power Delivery*, vol. 37, no. 4, pp. 2775–2786, Aug. 2022.

[10] L. Liu and Y. Lu, "A Protection and Control Coordinated Strategy for MMC-VSC HVDC System with Single AC Outgoing Line," in *2023 5th International Conference on Power and Energy Technology, ICPET 2023*, Institute of Electrical and Electronics Engineers Inc., 2023, pp. 394–399.

[11] Y. Gong, Q. Hao, L. Ding, and D. Li, "Fault Analysis of Offshore AC System at MMC-HVDC Connected with Offshore Wind Farm," in *2023 6th International Conference on Energy, Electrical and Power Engineering, CEEPE 2023*, Institute of Electrical and Electronics Engineers Inc., 2023, pp. 754–760.

[12] "VDE-AR-N 4120:2015-01: Technical Connection Rules for High Voltage," 2015.

[13] "THE GRID CODE ISSUE 5," 2017.

[14] C. Brantl *et al.*, "D2.4: Requirement recommendations to adapt and extend existing grid codes." [Online]. Available: www.promotion-offshore.net

[15] "Commission Regulation (EU) 2016/ 1447 - of 26 August 2016 - establishing a network code on requirements for grid connection of high voltage direct current systems and direct current-connected power park modules."

[16] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, "Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems," 2016. [Online]. Available: www.wiley.com.