Implementation and Evaluation of a Unified Grid Forming-Following Controller for BESS-IBR Systems

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***Abstract*—In this work, the Unified Grid Forming-Following (UGFF) controller for inverter-based resources (IBR) is proposed, which is a robust generic control framework that integrates both grid-forming (GFM) and grid-following (GFL) algorithms. The controller determines the rotational speed and resulting angle reference through the combination of a Power Synchronization Loop (PSL) and a Phase Locked Loop (PLL). The calculation of the d- or q- axis current reference is carried out within a single Proportional-Integral (PI) controller, which regulates two error signals respectively from the conventional GFM and GFL controllers. The relative contribution of error signals is determined by a Forming-Following Coefficient (FFC), which is designed to give seamless transitions. Specifically, FFC = 0 indicates pure GFL control, and FFC = 1 for pure GFM. The proposed UGFF is implemented in hardware controller to regulate a Battery Energy Storage System (BESS) modelled on a real-time Electromagnetic Transients (EMT) platform, forming a Hardware-in-loop (HIL) configuration. Simulation results demonstrate that with proper selection of FFC value, the UGFF can exhibit faster, and more resilient post-fault recovery compared to the GFM or GFL controllers.**

***Index Terms*— Unified Grid Forming-Following (UGFF), inverter-based resources (IBR), Battery Energy Storage System (BESS), Hardware-in-loop (HIL), Electromagnetic Transients (EMT) simulation.**

I. INTRODUCTION

With the increasing integration of renewable energy, modern power systems are increasingly dominated by inverter-based resources (IBRs), which typically employ either grid-following (GFL) or grid-forming (GFM) converters [1-4], sometimes supplemented by battery storage on the dc side.

GFL controllers rely on a Phase-Locked Loop (PLL) to track system frequency. A typical GFL control structure is shown in Fig. 1, consisting of an external loop and an internal current loop. GFL-IBRs face operational challenges in low Short Circuit Ration (SCR) systems [1].

In contrast, the GFM controller – which has attracted significant recent attention - employs a Power Synchronization Loop (PSL) to generate the frequency and phase angle at the converter terminals. In this scheme, the IBR adjusts its frequency in response to active power supply changes. A typical grid-forming (GFM) control block [2-4] is shown as in Figure 2, including an external PSL and Q/V loop, along with the internal voltage and current loops. The PSL is a droop controller consisting of a low pass filter '*LPF*' and the gain coefficient 'K_p'. GFM systems can exhibit the same limitations as SGs, particularly low frequency power-angle oscillations (< 10Hz) when connected to high SCR systems [5]. Furthermore, the GFM generally has a slower dynamic response to system faults compared to its GFL counterpart.

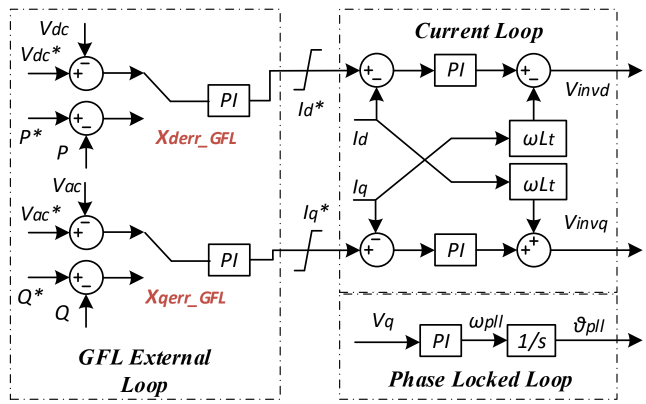

Figure 1. A typical grid-following controller

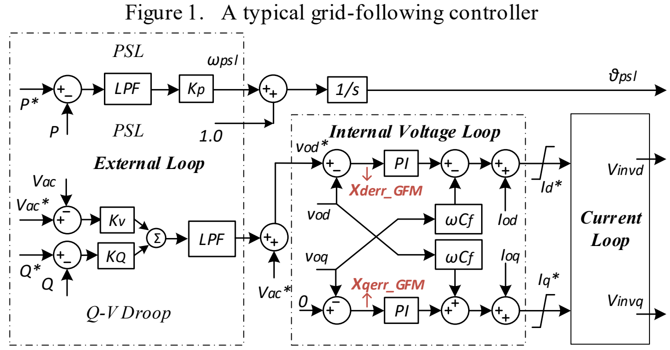

Figure 2. A typical grid-forming droop controller

Several studies have attempted to combine the strengths of both GFM and GFL control strategies. One approach is to equip IBRs with both controllers: at any instant, one controller governs the system while the other remains on standby [6]. A seamless transition can be attempted by resetting the PI controller states at the instant of mode switching. However, this approach has trade-offs: converters lack grid-synchronization capability in GFL mode and may respond slowly to transient faults when in GFM mode. Moreover, the transition cannot remain seamless under varying operating points.

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Another approach is the adaptive hybrid GFM and GFL controller [7-9], in which both PSL and PLL contribute to generating frequency and phase angle. A Weighting Coefficient (WC) between 0 and 1 determines the relative contributions. When WC is 1.0, the PSL solely decides the phase reference; and when WC is 0.0, the phase reference comes entirely from the PLL. To prevent large disturbance after adjusting WC value, the internal voltage loop is typically designed as a coupled loop, e.g., damping control loop or susceptance control loop [7-10]. These coupled loop implementations differ across the above studies, indicating the need for further investigation and standardization. In all cases, controllers with WC = 1.0 deviate from a traditional GFM controller, and controllers with WC = 0.0 do not correspond to a GFL controller. The resulting behavior of the controllers in [7-10] has not been investigated as thoroughly as the typical GFM and GFL schemes.

This paper proposes a Unified Grid Forming-Following (UGFF) that extends the hybrid control algorithms and ensures seamless online mode transitions. It determines converter frequency with a hybrid angle tracker incorporating both PSL and PLL, while the ac voltage is regulated with a Q/V droop. The internal voltage loop has two PI regulators receiving weighted inputs: one corresponding to the input of GFM internal voltage loop, and the other from GFL external loop. A coefficient - Forming-Following Coefficient (FFC) – is used as weighting factor. When FFC is 0.0, the UGFF is a standard GFL controller, and the decoupled terms are additionally included to the external voltage loop controller; and when FFC is 1.0, it is identical to a typical GFM controller. Thus, the UGFF provides a well-defined bottom-line behavior in worst scenarios that matches traditional GFM or GFL controllers when the FFC is set to 1.0 or 0.0, respectively.

The designed UGFF is implemented on a hardware platform and applied to regulate a Battery Energy Storage System (BESS) in a real-time Electromagnetic Transient (EMT) platform, forming a Hardware-in-loop (HIL) configuration. Experimental results of FFC step changes demonstrate smooth transitions without introducing noticeable disturbance to the network. Simulations further show that a controller with FFC value of 0.5 achieves improved performance compared to pure GFM controller (FFC = 1.0) or pure GFL controller (FFC = 0.0) following a three-phase grounding fault, or a phase angle jump. The on-line dynamic adjustment of UGFF allows operators to flexibly tune system characteristics to meet regulatory and operational requirements.

II. UGFF MODELING AND IMPLEMENTATION

Figure 3 presents the overall control block of the proposed UGFF. Broadly, it consists of three control loops: 1) an external loop – a hybrid angle tracker and Q/V droop loop [7-9] that determines the phase angle and ac voltage reference; 2) an internal voltage loop emulating the decoupled behavior of the filter capacitor to generate current reference signals; and 3) an internal current loop which emulates the dynamics of the ac inductor providing voltage reference signals.

A. External hybrid angle tracker and Q-V droop

The hybrid angle track decides the speed reference of the converter from two parts: a PLL tracking the system frequency, and a PSL establishing the converter frequency. To enhance the high-frequency response in pure GFM operation, a Transient Voltage Tracker (TVT) based on fast Internal Voltage Source (IVS) control [11] is incorporated into the PSL.

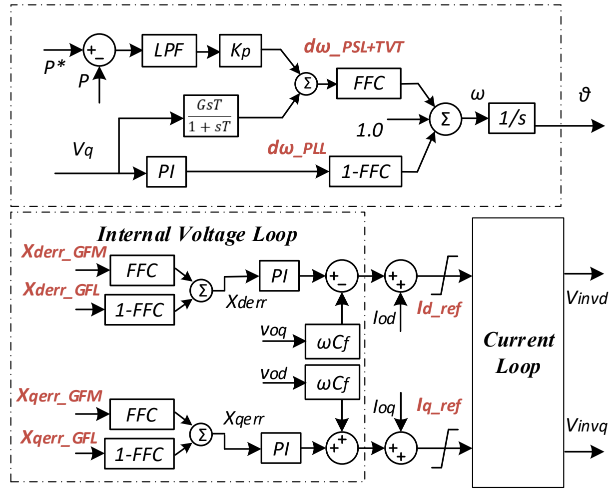

Figure 3. Unified Grid Forming-Following (UGFF) Controller

The value of FFC is multiplied to the PSL output, and the value of (1-FFC) is multiplied to the PLL output. The equation deciding the speed signal is:

$$\omega = FFC \cdot \omega_{PSL+TVT} + (1 - FFC) \cdot \omega_{PLL} + 1.0 \quad (1)$$

The Q-V droop is the same as the GFM controller on Fig. 2 and is not plotted in Fig. 3.

B. Internal voltage control loop

In the internal voltage control loop, the input signals for both the conventional GFM and GFL are considered. Like the external control loop, their relative contributions are weighted by the FFC value. Specifically, the two PI regulators receive the error signals from both GFL and GFM, X_{derr_GFL}, X_{qerr_GFL} X_{derr_GFM}, X_{qerr_GFM}, as shown in Fig. 1-2 that:

$$\begin{cases} X_{derr} = FFC \cdot X_{derr\_GFM} + (1 - FFC) \cdot X_{derr\_GFL} \\ X_{qerr} = FFC \cdot X_{qerr\_GFM} + (1 - FFC) \cdot X_{qerr\_GFL} \end{cases} \quad (2)$$

Since the combined signals are directly supplied into the two PI controllers, adjusting the FFC parameter does not need additional measures to prevent a sudden change in the PI outputs. This contrasts with seamless or hybrid controllers in previous studies, which require resetting the PI states prior to adjusting FFC. A decoupling term is added to the PI output to generate the d-axis and q-axis current reference signals.

C. Interal current loop

The internal current loop consists of two PI regulators that act on the error signals of the d- and q- axis currents. A decoupling term is included to capture the dynamic behavior of the ac inductor.

D. Physical implementation of UGFF

The UGFF controller was physically implemented on a hardware processor card (PB5) including two Freescale MC7448 RISC processors operating at 1.7 GHz [12]. The controller regulates a Battery Energy Storage System (BESS) simulated in a real-time digital simulator, forming a Controller Hardware-in-loop (CHIL) configuration.

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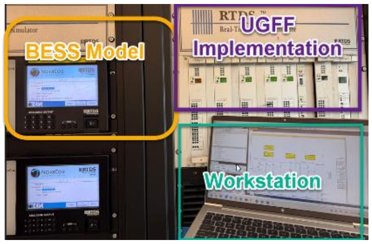

Figure 4. UGFF controller and CHIL simulation setup

III. MODELLING OF BESS ELECTRIAL SYSTEM

The BESS system is modelled in a real time EMT simulator, with its configuration [13] illustrated in Fig. 5. The dc side battery is connected to the low-voltage ac side via a boost converter and a dc-ac converter. The nominal battery voltage is 0.43 *kV,* while the dc bus voltage is 0.8 *kV*. Under steady state conditions, the battery delivers 1.0 *MW* + j 0.03 *Mvar* power to ac side.

At the converter terminal, the ac voltage is 0.45 *kV* (line-to-line RMS) and is stepped up to 35 *kV* by a transformer connecting to the PCC bus. A PQ load of 0.5 *MW* + j 0.0 *Mvar* is connected to the PCC. The PCC bus is further linked to a 220 *kV* grid through another step-up transformer, sending 0.5 MW of active power to the ac Thevenin source. The Short Circuit Ratio (SCR) of the ac system is 2.7. The reactive power flows to PQ load and to ac Thevenin source is minimal. The nominal frequency is 50 Hz, and the simulation timestep is 50 *us*.

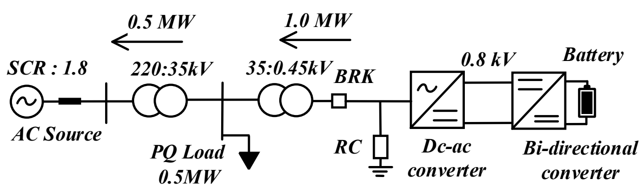

Figure 5. Configurtion of simulated BESS system

A. Modelling the batteries

In the EMT simulation, the battery in the dc side uses a piecewise linear battery model with parameters as in Table. 1.

TABLE I. BATTERY PARAMETERS

Single Cell Parameters	Value	Parameters	Value
Nominal Voltage	*0.0036kV*	*Initial voltage*	*1.09 pu*
Rated Capacity	*0.0167kA*hr*	*Series Cell number in a stack*	*111*
1h capacity loss at nominal current	*20%*	*Parallel stack number*	*200*
Initial SOC	*90%*		

B. Bi-directional and dc-ac converter

The bi-directional and the dc-ac converter connect the battery to the dc bus, and subsequently to the ac converter terminal. In the simulator, the converter is modelled using descriptor state space equations, referred to as a 'Universal Converter Model' [14-15] which receives the converted firing pulses as input to ensure simulation accuracy. The parameters of the two converters in the EMT simulation are shown in Table. 2.

TABLE II. BI-DIRECTIONAL AND DC-AC CONVERTER PARAMETERS

Bi-directional converter	Value	Dc-ac converter	Value
Inductor	*2.85e-4 H*	*Inductor*	*1.46e-4 H*
Low voltage side capacitor	*5000 uF*	*Dc capacitor*	*16000 uF*
High voltage side capacitor	*16000uF*	*Switching frequency*	*2000 Hz*
Switching frequency	*5000 Hz*	*Filter capacitor*	*646 uF*
		Filter resistor	*0.118 ohm*

C. Controller for the bi-directional converter

As shown in Fig. 6, one PI controller generates the boost converter's current order 'I_{dc}* to achieve the desired dc voltage, and a second cascaded PI controller to generate duty cycle.

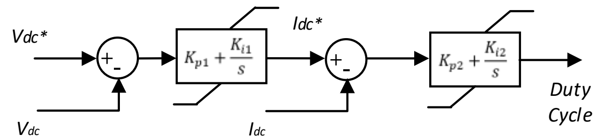

Figure 6. Control Scheme of the bi-directional converter

IV. SIMULATION RESULTS AND VALIDATION

To validate the proposed UGFF, three operating scenarios are examined in this study, i.e., 1) seamless adjustment of FFC value with SCR = 2.7, 2) three-phase fault in strong system - SCR = 10, and 3) three-phase fault in weak system - SCR = 2.

A. Seamless adjustment of FFC value

This experiment validates the ability of the UGFF to achieve seamless transitions of converter behaviors when adjusting FFC value. To demonstrate this capability under the most extreme conditions, the value of FFC is adjusted from 0.0 to 1.0, i.e., from pure GFL mode to pure GFM mode, at time t = 0.2 seconds; and back to 1.0 (pure GFL mode) at t = 1.2 seconds. The result waveforms are shown on Fig. 7.

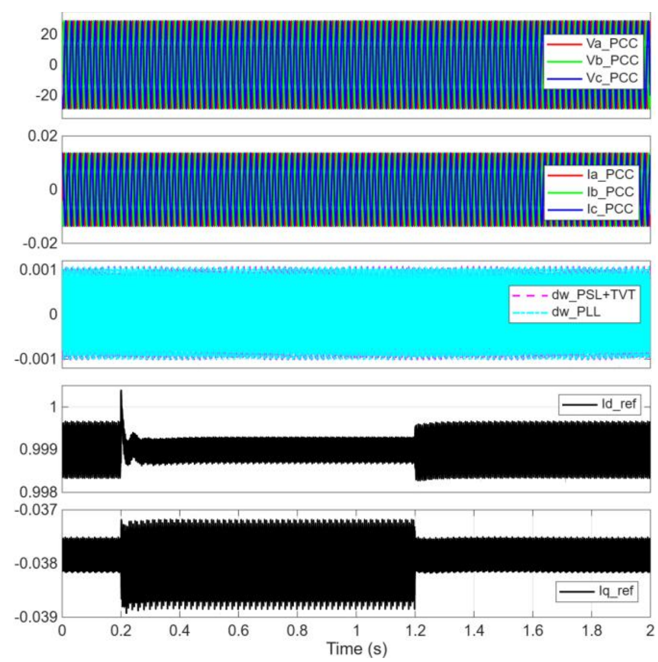

Figure 7. FFC adjustment from 0.0 to 1.0 and then back to 0.0

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The first and second subplots are the three-phase voltage and current, *'V_pcc'* and *'I_pcc'*; the third to fifth subplots specifically show the unified controllers' speed outputs, i.e., *'dw_PSL+TVT'* and *'dw_PLL'*, as well as d- and q- axis current reference *'Id_ref'* and *'Iq_ref'*, all of which was shown in Fig. 3. The observation of the above system signals and control signals clearly confirms the seamless transition when adjusting FFC value.

B. Three-phase fualt at PCC bus for strong ac system

In this subsection, an experiment is conducted to evaluate UGFF behavior following a three-phase ground fault at the PCC bus. In this case, the system SCR = 10. Fig. 8-10 shows the post-fault waveforms for three cases of FFC = 0.0, 1.0, 0.5 in four subplots, i.e., RMS voltage *'Vpcc_RMS'*, RMS current *'Ipcc_RMS'*, active power of PCC bus *'Pac'*, and the speed output signals *'dw_PSL+TVT'* and *'dw_PLL'*.

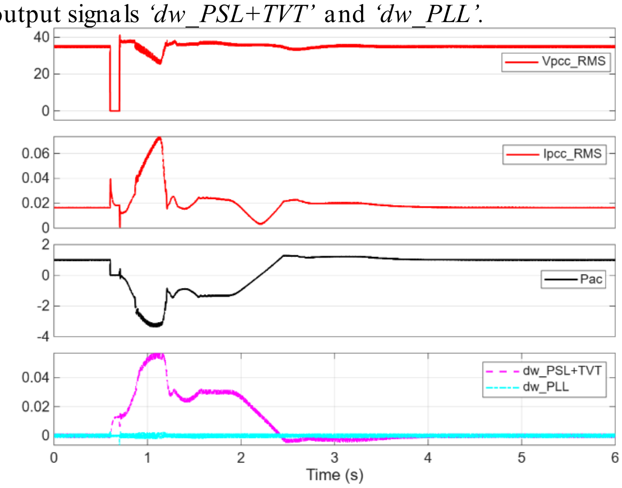

Figure 8. Post-fault performance for pure GFL mode (SCR = 10)

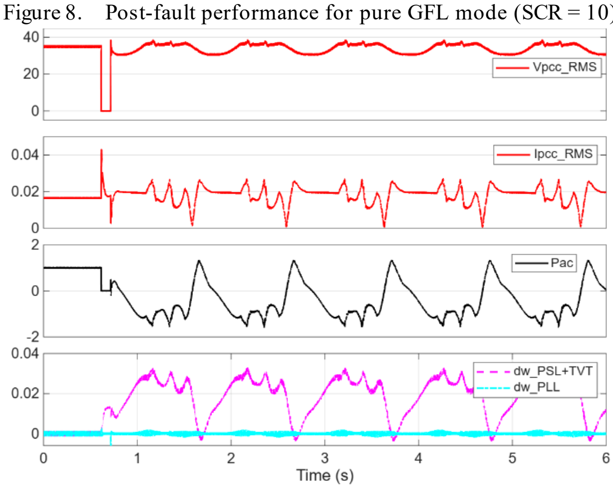

Figure 9. Post-fault performance for pure GFM mode (SCR = 10)

The result shows that the UGFF controller with FFC = 0.5 has the most resilient recovery behavior following fault bus, that the speed and current reference signals convergences faster than the pure GFL controller (FFC = 0.0), whereas the pure GFM mode (FFC = 0.0) fails to recover. This agrees with the previous conclusion that GFM converters face challenges connecting a system with high SCR value [5][8].

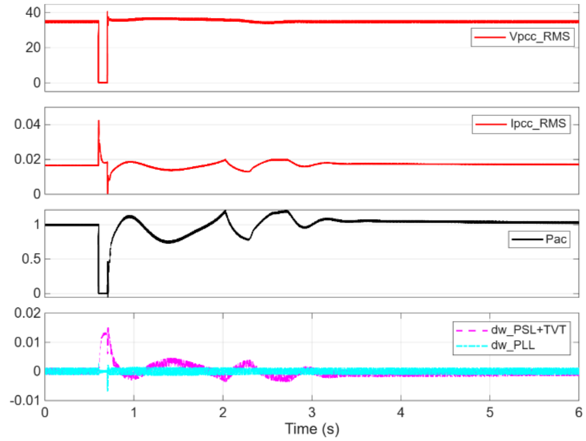

Figure 10. Post-fault performance for FFC = 0.5 (SCR = 10)

C. Three-phase fault at PCC bus for weak ac system

In this subsection, the three-phase fault is conducted in a weak system with SCR = 2. Fig. 11-13 shows the post-fault waveforms for three cases of FFC = 0.0, 1.0, 0.5. Like the strong ac system, the UGFF controller with FFC = 0.5 shows the most robust recovery procedure that the waveforms suffer least transient disturbance and fastest convergence to steady state.

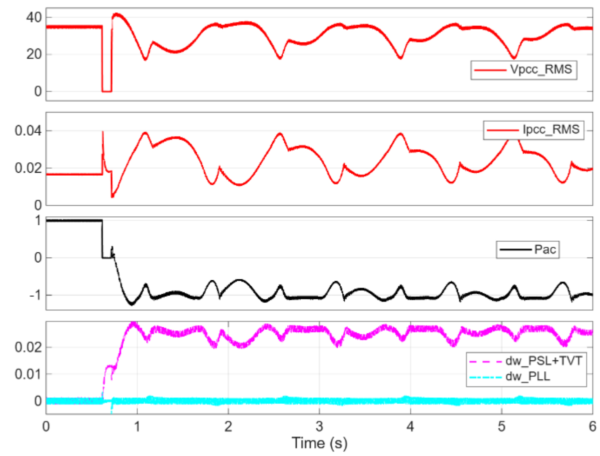

Figure 11. Post-fault performance for pure GFL mode (SCR = 2)

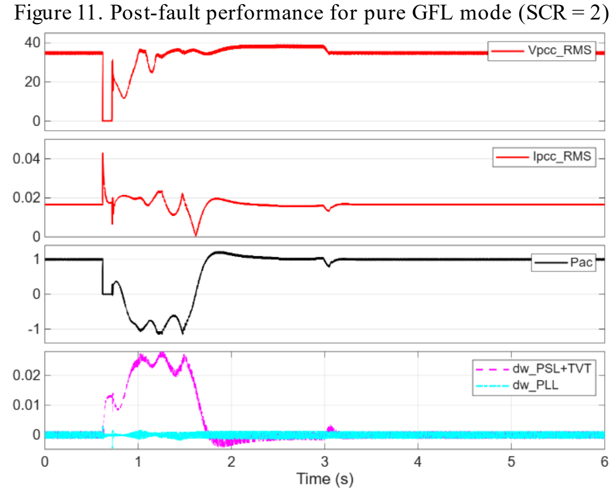

Figure 12. Post-fault performance for pure GFM mode (SCR = 2)

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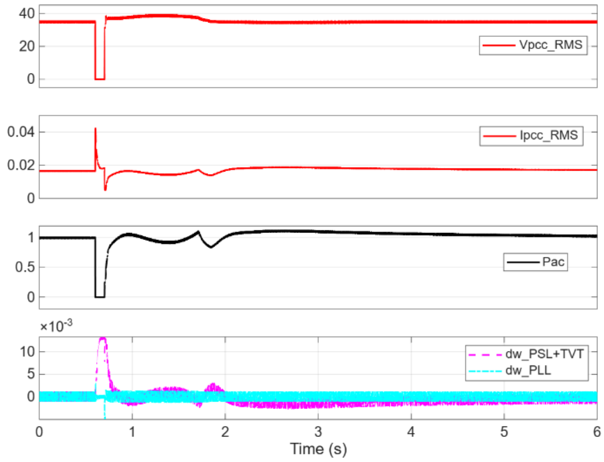

Figure 13. Post-fault performance for FFC = 0.5 (SCR = 2)

D. *Recovery time as function of FFC value for strong and weak ac systems*

The post fault recovery performance is further quantified by measuring the recovery time of active power, defined as the duration required for the active power at the PCC bus to return and remain within the bounds of 0.8 pu to 1.2 pu following a fault event, as shown in Fig. 14. The dot line part in the curve indicates that the system becomes unstable after fault. For a strong system (SCR = 10), a better recovery time is presented at first when FFC increases (value 0.0 to 0.6), however, fails to recover when FFC further increases above 0.7. For a weak system (SCR = 2), the system cannot recover with pure GFL mode (FFC = 0.0), and shows best behavior when FFC = 0.5, which is a recovery time of 0.14 seconds. These results highlight the flexibility of the UGFF controller and its ability to be fine-tuned for different grid conditions to achieve optimal dynamic performance.

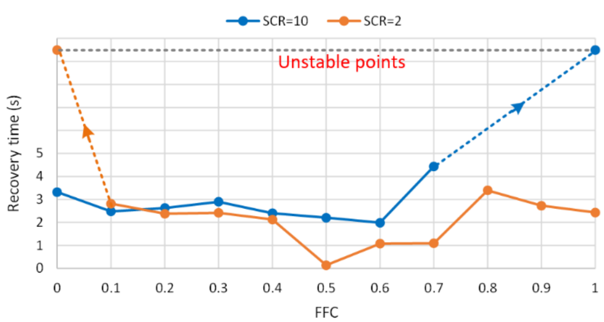

Figure 14. Active power recovery time following fault events for varying FFC

V. Conclusions

In this work, a Unified Grid Forming-Following (UGFF) controller is proposed building on the concepts from seamless transition and hybrid control strategies. It can operate as a pure conventional GFM (FFC = 1) or GFL (FFC = 0, with an additional decoupled term in the external voltage loop). What is interesting is that it can simultaneously combine orders generated by individual GFM and GFL control loops by selecting FFC to be between 0 and 1. It also allows seamless dynamic adjustments based on the operating conditions, which can help satisfy regulatory requirements, maximize power transfer capability and enhance transient stability.

The effectiveness of UGFF is validated via CHIL simulation regulating a BESS system. The results demonstrate: 1) stable and reliable transitions across different FFC values; and 2) a resilient post-fault regulation capability of UGFF with proper FFC value selection, where the controller with FFC = 0.5 provides the fastest and most robust recovery results compared to pure GFM or GFL controls; 3) that the recovery time as an indicator can be used to determine the optimized value of FFC for different system conditions and for dynamic adjusting during operating.

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