From Regulation to Reality: A Verified, Vendor-Agnostic Control Architecture for Mandatory FCR-Prequalification of Limited-Energy Storage in Germany

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***Abstract*—'Powering the Digital Era' requires new methodologies to translate complex regulatory requirements into deterministic, machine-executable code. Limited energy storage systems delivering frequency containment reserve must meet stringent requirements defined by the European System Operation Guideline and the German prequalification process including dynamic state-of-charge limits, timed operating mode transitions, alert-state detection, and reserve mode operation based on a five-minute moving average of the grid frequency. This paper presents a novel, vendor-agnostic, modular control architecture that formalizes these requirements into verifiable digital subsystems. The proposed controller was implemented on Siemens Energy's Omnivise T3000 industrial controller, tested in simulation and validated using controller-hardware-in-the-loop. Results confirmed regulatory compliance and suggested ways to resolve industrial controller limitations, such as moving average buffer depth, through systematic workarounds. By bridging the gap between policy and implementation, this work provides a transparent reference for regulators and operators, advancing the digitalization of ancillary service provision.**

***Index Terms*-- Battery Energy Storage, Compliance, Frequency Containment Reserve, Industrial Controller, Prequalification.**

I. Introduction

The decarbonization of power systems, driven by the integration of inverter-based resources (IBRs) reduces system inertia and amplifies vulnerability to frequency disturbances [1], [2]. This evolution makes the stable and reliable operation of digital era grids a paramount concern. Battery Energy Storage Systems (BESS) provide rapid and accurate power adjustments, making them critical for delivering Frequency Containment Reserve (FCR), the primary automatic response to frequency deviations.

At the European level, the System Operation Guideline (SOGL) [3] specifies proportional droop behavior, activation characteristics, and continuous energy reserve availability. The German prequalification (PQ) process [4] refines these requirements with explicit, quantifiable performance targets: FCR activation proportional to frequency deviations, strict tolerances on power fluctuations, and additional provisions for limited energy resources (defined by the regulation's requirement for mandatory transition to a diminished "reserve mode" upon breaching the dynamic SOC boundaries, preventing full discharge/charge), including the definition of an alert state, state-of-charge (SOC) operating ranges, and a reserve mode.

Industrial providers meet these requirements in practice, but their implementations are embedded in proprietary platforms. The lack of transparency leaves regulators and researchers without a reference for testing, auditing, and standardization. This paper presents the first vendor-agnostic and modular framework that transparently translates textual provisions from [4] into machine-verifiable control logic. The proposed solution is validated on industrial control hardware, thereby contributing to an open and digitalized ecosystem for ancillary services. This work directly contributes to the conference's focus on "Operating the Grid: by ensuring robust, compliant and verifiable FCR provision from BESS" and "High Penetration IBR management: by enhancing the reliability of BESS as a key IBR providing essential grid services".

The key contributions of this work are: (1) a novel, vendor-agnostic, and modular control architecture that provides a transparent, clause-by-clause mapping of complex FCR prequalification text [4] to verifiable software modules, (2) a practical validation of the logic via Controller-Hardware-in-the-Loop (CHIL) tests on an industrial platform (Siemens Energy Omnivise T3000), including solutions for real-world hardware constraints (e.g., cascaded averaging for buffer limits) and (3) a demonstrated pathway for digitizing and standardizing ancillary service compliance, bridging the gap between policy and deterministic implementation.

II. Literature Review

Research on BESS for frequency regulation has largely focused on sizing and operational strategies. Refs. [5] and [6] optimized battery sizing and SOC management for FCR delivery, identifying economic trade-offs but not publishing detailed control logic. Ref. [7] and [8] analyzed recovery strategies for limited-energy resources, highlighting the importance of maintaining SOC margins but stopping short of deterministic implementations. Ref. [9] presented multi-year

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operational insights from the M5BAT project, demonstrating technical feasibility but without a modular regulatory mapping. Ref. [10] investigated operating strategies for FCR delivery using historic frequency data to validate their test results.

Policy studies, such as those from Fraunhofer [11], interpret European regulations and their national applications, while Controller- and Power- Hardware-in-the-Loop (CHIL and PHIL respectively) experiments are widely used in testing distributed energy resources [12].

What remains absent in the literature is a reproducible framework that formalizes these provisions into machine-verifiable modules, validated with historic frequency signals and adapted for industrial control hardware. This paper is the first to bridge that gap by documenting a vendor-agnostic, transparent implementation of FCR prequalification requirements.

III. Regulatory Compliance Requirements

BESS units participating in FCR must satisfy a strict set of technical requirements (defined in [4]) designed to ensure that limited-energy resources contribute reliably under all system conditions. These requirements can be distilled into a set of functional specifications, which form the foundation of the proposed modular control architecture. Table I summarizes how each requirement is mapped into the proposed architecture and validated through Simulink and CHIL tests.

TABLE I. Compliance Mapping: Regulatory Requirements to Architecture

Requirement	Proposed Module	Validation Evidence
Alert state detection under defined magnitude/duration thresholds	Alert state detection	Correct activation /deactivation observed (Fig. 2b)
Dynamic SOC boundaries ensuring energy availability	Dynamic SOC Limits Calculator	SOC thresholds breach correctly detected (Fig. 2b/d)
Reserve mode activation and deactivation based on SOC level and alert state status	State transition machine	Mode transitions and 5-min ramps observed (Fig. 2a/b/c)
A mandatory deterministic 5-min ramp transition period between normal and reserve modes		Transition ramps observed (Fig. 2b/c)
5-min moving average for reserve operation	Frequency blending	Five-minute averaging verified during reserve mode operation (Fig. 2a/b/c)
Blending of raw and 5-min moving averaged frequency during transitions		Smooth weighted blending confirmed in transition periods (Fig. 2a/c)
Provision of a proportional power response (P(f)) to all frequency deviations	Power setpoint computation	Droop response confirmed (Fig. 2a/c)

IV. Modular Control Architecture

The proposed architecture, shown in Fig. 1, translates the requirements from Table I into five interconnected and auditable modules. This modular approach ensures clarity, simplifies the validation of individual compliance points, and enhances the robustness and maintainability of the system. The architecture is designed to seamlessly integrate with higher-level Energy Management Systems (EMS) and grid operator commands while providing deterministic, regulation-compliant performance at the converter level.

The core function of the architecture is to translate the measured grid frequency and the internal battery SOC into a compliant FCR power setpoint (P_{FCR}). The system is governed by a state-based logic that transitions between distinct operational modes: normal, entry, reserve, and exit, based on stringent conditions defined by [4]. The five key modules are the alert state detection, dynamic SOC limits calculator, state transition machine, frequency blending and power setpoint computation.

1. **Alert State Detection** This module is the primary trigger for the controller's state transition logic, ensuring the storage system prepares for and responds to significant frequency events in a regulation compliant manner. The system's logic is based on a multi-threshold time duration principle. The input is the absolute value of the measured grid frequency deviation, $|\Delta f|$. The system generates an *Alert State* flag that becomes active (TRUE) when any of the following three conditions are met: (i) instantaneous trigger: $|\Delta f| \geq 200$ mHz for a single sample, (ii) sustained deviation trigger 1: $|\Delta f| \geq 100$ mHz persists continuously for a duration of 5 minutes and, (iii) sustained deviation trigger 2: $|\Delta f| \geq 50$ mHz persists continuously for a duration of 15 minutes. Exit from the alert state occurs when the frequency deviation falls below 50 mHz. The three triggers are directly transcribed from the regulatory thresholds in [4]. They enable discrimination between transient noise, sustained disturbances, and critical events.

2. **Dynamic SOC Limits Calculator:** This subsystem calculates dynamic operational boundaries for the battery's SOC based on (1). Its primary function is to determine when the SOC has drifted outside its permissible operating range, thereby triggering a transition to reserve operation (by generating Boolean outputs "SOC Out of Bounds" that command the state transition machine to initiate transition, assuming other reserve entry/exit conditions are simultaneously met) to prevent a complete loss of FCR capability.

$$C_{UG} = \frac{(P_{VL} * \Delta t_{FAT})}{E_{usable}}, C_{OG} = 1 - C_{UG} \quad (1)$$

C_{UG} and C_{OG} are the lower and upper SOC thresholds expressed in p.u. for reserve operation activation; P_{VL} is the marketable power in MW and E_{usable} is the usable energy capacity of the BESS in MWh. These regulation-derived thresholds C_{UG} and C_{OG} operate on the market-nominated E_{usable}. In a full system implementation, a higher-level EMS would dynamically adjust E_{usable} to reflect real-time physical constraints (e.g., temperature, degradation, maintenance flags), ensuring the FCR controller always operates within the BESS's safe physical boundaries. The thresholds for reserve operation activation (C_{UG}, C_{OG}) and the mandatory transition period are defined based on the

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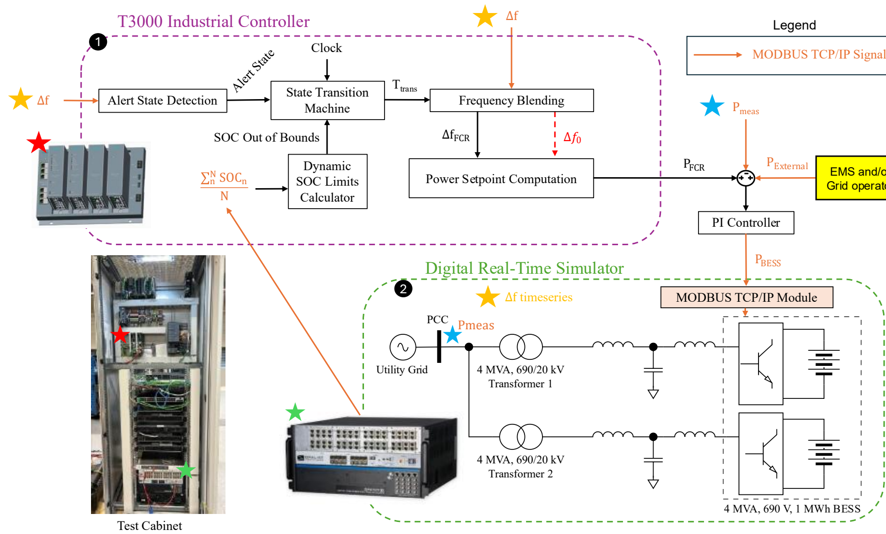

Figure 1. CHIL test setup showing a block diagram representation of the proposed vendor-agnostic modular architecture. Modules are designed to map directly to specific clauses in [4]. T3000 Industrial Controller runs FCR control logic and communicates setpoint to inverters in OPAL-RT.

full activation time of automatic Frequency Restoration Reserve (aFRR), where Δt_{FAT} = 5 minutes [4]. This deliberate linkage ensures that an energy-limited FCR unit's transition to a diminished state of operation occurs over a standardized and predictable duration. It provides a critical grace period, allowing the grid's secondary control reserves (aFRR) time to fully activate and compensate, thereby maintaining system stability and avoiding a sudden loss of active power support.

3. **State Transition Machine:** This module is the central coordinating logic of the FCR controller. It implements the mandatory, 5 minutes transition period between operational states in response to triggers from the dynamic SOC limits calculator and alert state detection modules. It ensures the system behaves deterministically and complies with the strict timing requirements of the prequalification process. Transition from normal to reserve operation is activated by the breach of C_{UG}/C_{OG} and the presence of an alert state while a transition back from reserve to normal is activated only when both activating conditions are off. The core innovation of this module is the generation of a continuous transition variable T_{trans} ∈ [0,1] following (2). T_{trans} ramps linearly from 0 to 1 over exactly 5 minutes (Δt_{FAT}) during entry transition, and from 1 to 0 during exit transition. T_{trans} signal is the key enabler for the seamless blending of frequency response characteristics between states, avoiding any disruptive steps in the commanded power.

$$\mathrm{T_{trans}}(\mathrm{t}) = \mathrm{T_{trans}}(t_{\mathrm{switch}}) - \frac{(-1)^R}{\Delta \mathrm{t_{FAT}}}(t - t_{switch}) \tag{2}$$

where $T_{trans}(0)$ is 0, t_{switch} is the time of system transition, R is the status variable for unit operation (R is 1 when reserve mode operating conditions are met while R is 0 when normal mode operating conditions are met).

4. **Frequency Blending:** This system generates the appropriate deviation signal for the power calculation depending on the operational state commanded by the state transition machine. It ensures that the BESS's response to frequency deviations complies with the different requirements for normal and reserve operations. The system has two primary processing paths: (i) normal operation path: the measured frequency deviation Δf is used directly and (ii) reserve operation path: Δf is processed to create a zero-mean output, $\Delta f_{zero\ mean}$. This is achieved by subtracting a moving average of Δf over a window equal to Δt_{FAT} from Δf, as per (3).

$$\Delta \mathrm{f_{zero\ mean}}(\mathrm{t}) = \Delta \mathrm{f}(\mathrm{t}) - \frac{1}{\Delta \mathrm{t_{FAT}}} \sum_{\mathrm{i}=0}^{\Delta \mathrm{t_{FAT-i}}} \Delta \mathrm{f}(\mathrm{t}-\mathrm{i}) \tag{3}$$

The system's output is not a simple switch between these two paths. During the transition states, the final output $\Delta f_{FCR}(t)$ is a weighted blend of the normal and reserve signals, as mandated by (4).

$$\begin{aligned}\Delta \mathrm{f_{FCR}}(\mathrm{t}) = \Delta \mathrm{f_{zero\ mean}}(\mathrm{t}) * \mathrm{T_{trans}}(\mathrm{t}) \\ + \left(1 - \mathrm{T_{trans}}(\mathrm{t})\right) * \Delta \mathrm{f}(\mathrm{t})\end{aligned} \tag{4}$$

This module implements the precise frequency response requirements for reserve operation and transition blending.

5. **Power Setpoint Computation:** This final subsystem calculates the actual power setpoint (P_{FCR}) that is sent to the power converter. It translates the processed frequency deviation signal into megawatt value, adhering to the droop characteristic and the unit's prequalified power limits. The core calculation is based on the standard droop formula for FCR by applying (5).

$$\mathrm{P_{FCR}} = \Delta \mathrm{f_{FCR}}(\mathrm{t}) * \frac{-\mathrm{P_{PQ}}}{0.2\ \mathrm{Hz}} \tag{5}$$

P_{PQ} is the prequalified power of the unit, and -0.2 Hz is the droop slope: meaning full power is commanded at a 200 mHz deviation. The result of this calculation is passed through a final saturation block, which clamps the output to the symmetrical limits of $\pm P_{PQ}$. This ensures that the unit never exceeds its prequalified capacity, a fundamental requirement for safe and compliant operation. The output P_{FCR} is a stable, compliant, and limited power setpoint ready for execution by the inverter. This module embodies the fundamental *P(f)* droop characteristic required by [3] and ensures the output remains within the prequalified power limits, a key tenet of the entire prequalification process.

This modular design ensures each regulatory clause is mapped to a specific, testable software block, fulfilling the need for transparency and auditability.

V. Industrial Implementation and Challenges

The Siemens Omnivise T3000 [13] is a standard industrial automation controller used in energy applications, featuring deterministic execution cycles, IEC 61131-3 programming, and various communication protocols. Implementing the architecture and FCR logic on the controller revealed a few hardware limitations which were resolved, and which demonstrated the framework's practicality and adaptability.

1. **Five-Minute Moving Average Buffer Limit:** One of the most critical challenges concerned the moving average calculation required for reserve mode operation. The regulation specifies that frequency deviations in reserve mode must be referenced against a five-minute moving average. At a 20 ms sampling time, this would require storing 15000 samples, far exceeding the T3000's buffer capacity of 256. An initial workaround was devised by compressing 60 consecutive samples (1.2 s of data) into a single intermediate average and then storing 250 of these intermediate values to reconstruct the required 300 s moving window. However, a second limitation emerged: the minimum achievable interrupt interval on the T3000 controller was 40 ms, not 20 ms. The scheme was therefore refined by averaging 30 samples at 40 ms (still representing 1.2 s of data) before feeding them into the 250-sample buffer. This cascaded averaging structure precisely reproduces a 5-minute moving average while remaining within the controller's hardware limits, ensuring that the reserve mode remains compliant with the regulatory definition.
2. **Deterministic Timing Using Computation Cycles:** To ensure strictly deterministic timing for all regulatory timing constraints, including state transitions and alert-state detection, the implementation avoids the controller's absolute time clock, which is susceptible to disruptive synchronization corrections. Instead, discrete integrator blocks are employed to count a fixed number of computation cycles. This method guarantees that the 5-minute transition ramps and the sustained frequency deviation checks (e.g., 5-minute and 15-minute timers) are based solely on the elapsed, deterministic execution time of the control logic. This approach renders the entire process immune to external clock synchronization artifacts, ensuring uncompromised regulatory compliance for all time-dependent functions.

These solutions exemplify a core principle: compress, cascade, or normalize where necessary, but always preserve the regulatory invariant. This makes the architecture both compliant and practical for today's industrial control environments.

VI. Key Results and Discussion

To evaluate the performance of the FCR control logic, a historic frequency event from January 2019 with dataset suggested in [4] by TenneT was used. The frequency deviation signal Δf was converted to a timeseries and sent to the FCR controller using MODBUS TCP/IP. As suggested by [4], a continuous recharging setpoint $P_{External}$ of 0.25 p.u. was added to P_{FCR} and passed to the closed-loop PI controller that generates the final setpoint P_{BESS} (by regulating the measured power P_{meas} at the Point of Common Coupling (PCC)). P_{BESS} is sent to the BESS model using MODBUS TCP/IP.

Fig. 2 shows the temporal relationship between frequency deviation, criteria for reserve mode of operation, transition to reserve mode, provision of PRL and SOC level of the batteries. Fig. 2 (a) shows the actual frequency deviation Δf in purple, the deviation from the new reference frequency $\Delta f_{zero\ mean}$ in green and the decisive factor for the actual provision frequency deviation Δf_{FCR} in orange. Associated with the same colors, Fig. 2 (c) shows the respective power values for a provision according to the corresponding frequencies; P_{ACT} is the provision based on Δf, P_{RES} is based on $\Delta f_{zero\ mean}$ and P_{FCR} is based on Δf_{FCR}. Fig. 2 (b) shows the alert state, SOC out of bounds and continuous transition variable T_{trans}. Fig 2 (d) shows the battery SOC and lower limit C_{UG} for the reserve mode. The controller correctly entered alert state, managed the battery SOC, and initiated a transition to reserve mode when required, all while maintaining compliant power output. Initially, the frequency deviation was within operational limits. No alert state existed. The continuous charging setpoint $P_{External}$ of 0.25 p.u. caused the SOC of the BESS to increase as seen in Fig. 2 (d). As soon as the frequency deviated by more than 200 mHz, the alert state was activated by the alert state detection module. Although the charging setpoint was still being added to the FCR power setpoint, the battery SOC dropped since full FCR power was being provided due to the activated alert state. The BESS continued to discharge until finally, despite the frequency starting to recover, the lower limit for reserve operation was reached. At this point, both the alert state and transition mode were active as seen in Fig. 2 (b). This initiated the ramp of the transition function T_{trans} from 0 to 1 within 300 s causing the BESS to switch to reserve mode. The divergence between Δf and Δf_{FCR} during this transition phase signifies the compliant activation of reserve mode where Δf_{FCR} is processed according to (4) in the frequency blending module. This divergence is also evident around t = 4760 s during the transition to normal mode. The system's total response latency (< 300 ms) was confirmed via CHIL to be well within the 2-second regulatory limit. The SOC recovered during the transition phase to above the reserve mode limit. Nevertheless, the BESS remained in reserve mode until the end of the alert state. The alert state was deactivated as soon as the frequency deviation was less than 50 mHz. The criteria for standby operation was no longer active, and the BESS transitioned from reserve mode to normal mode.

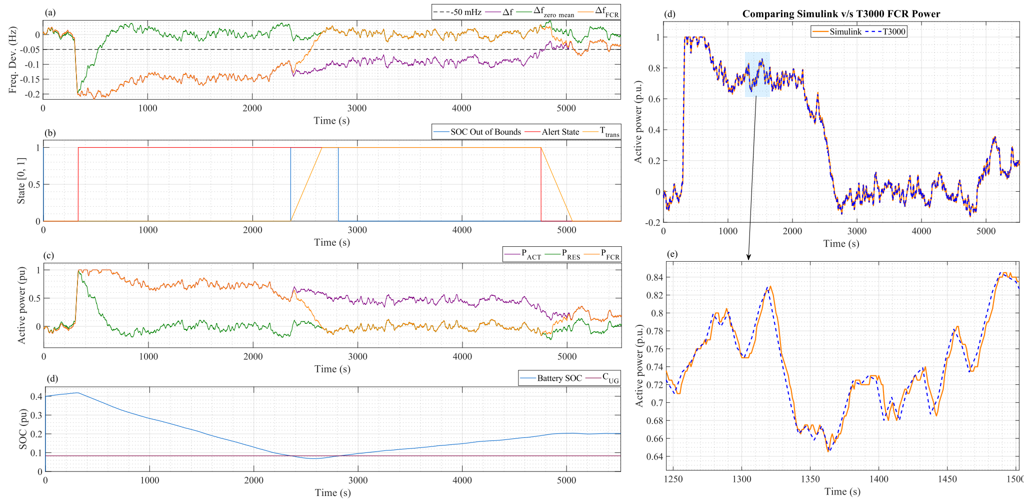

Figure 2. CHIL results using T3000 showing FCR provision based on test frequency signal from TenneT

T_{trans} decreased linearly from 1 to 0 within 300 s, which particularly affected the FCR frequency deviation.

Fig. 2 (d) and (e) show a comparison of the simulation results using Simulink tests and experimental CHIL tests. Negligible differences were observed, highlighting that the solutions adopted to resolve the hardware limitations were effective and preserved compliance with the FCR requirements. The CHIL test results confirm compliance across the critical, TSO-specified test scenario. The modular design enabled systematic unit and integration testing of each subsystem under varied inputs, verifying robustness prior to the full-system test shown.

VII. Conclusion

This paper presented a novel, vendor-agnostic, and modular control architecture that directly translates the text of the European System Operation Guideline and German prequalification process into deterministic, machine-verifiable code. By encoding activation dynamics, tolerance limits, alert states, SOC boundaries, and reserve mode averaging, the framework successfully bridges the gap between regulatory policy and digital implementation. Validation through Simulink and CHIL confirmed deterministic compliance, while deployment on a Siemens Energy Omnivise T3000 controller required systematic solutions to industrial hardware limitations, proving the framework's practical applicability. While the implementation was parameterized for the German market, the core methodology—modular decomposition of textual grid code into verifiable, deterministic software blocks—provides a transparent template adaptable to other international frameworks (e.g., FERC in North America, UK National Grid, or other ENTSO-E members). The architecture's parameterizable thresholds, timing logic, and droop characteristics facilitate this adaptation.

This work contributes to the "Digital Era" grid by providing a transparent, auditable reference for regulators, operators, and researchers, facilitating the standardization and secure integration of BESS providing critical ancillary services. Future work will extend this framework to include aFRR and manual Frequency Restoration Reserve (mFRR) products, integrate predictive SOC management for enhanced market participation, and explore harmonization across other European TSO prequalification processes.

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